Putting FPGAs to Work in Software Radio Systems

Third Edition

Technology

Resources

Products

Systems

Links

by

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FPGAs are becoming an increasingly important resource for software radio systems. This handbook introduces the basics of software radio followed by a brief review of the evolution of programmable logic technology which now offers significant advantages for implementing software radio functions.

An overview of Pentek’s GateFlow FPGA Design Resources is followed by product descriptions and finally by some software radio system examples that utilize FPGA technology.

We begin our discussion with the basic elements of a software radio receiver system.

The front end usually contains an analog RF amplifier and often an analog RF translator. This translates the high frequency RF signals down to a frequency that an A/D converter can handle. This is usually below 100 MHz and is often an IF output.

The A/D output feeds the digital downconverter (DDC) stage, which is typically contained in a monolithic chip which forms the heart of a software radio system.

Notice, that after the signal is digitized by the A/D converter, all further operations are performed by digital signal processing hardware.

Here we’ve ranked some of the popular signal processing tasks associated with software-defined radio (SDR) systems on a two axis graph, with compute Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs (Application Specific ICs) are usually chosen for these functions.

Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision making which are highly variable and often subjective.

Programmable general purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let’s temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.
As true programmable gate functions became available in the 1970’s, they were used extensively by hardware engineers to replace control logic, registers, gates and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters, giving the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.
Putting FPGAs to Work in Software Radio Systems

FPGAs: New Device Technology

- 500 MHz DSP Slices including multiplier and accumulator
- Up to 512 dedicated on-chip hardware MACs (multiplier / accumulators)
- Up to 200,000 Logic Cells
- On-chip 405 PowerPC RISC micro-controller cores
- Gigabit Ethernet Media Access Controllers
- Reduced power with core voltages near 1 volt
- Memory densities of over 10 million bits
- 500 MHz flexible memory structures for RAM and FIFOs
- Logic densities of over 10M gates
- Silicon geometries to 90 nanometers
- High-density BGA and flip-chip packaging
- On-board 11 GHz Switched Fabric serial interfaces
- Over 1200 user I/O pins
- Configurable logic and I/O channel interface standards

Figure 5

FPGAs: New Development Tools

- High Level Design Tools
  - Block Diagram System Generators
  - Schematic Processors
  - High-level language compilers for VHDL & Verilog
  - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - Faster compilers and simulators save time
  - Graphically-oriented debugging tools
- Third Party Cores
  - FPGA vendors are promoting 3rd party initiatives
  - Wide range of IP cores available

Figure 6

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks of up to 500 MHz, and lower core voltages to keep power and heat down.

About five years ago, dedicated hardware multipliers started appearing and now you'll find literally hundreds of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over 10 million gates result from silicon geometries shrinking down to 0.1 micron.

BGA and flip chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

To minimize some of the tricky timing work for hardware engineers, excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This can really save one hour of tedious troubleshooting, not only during design verification but also for production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.
Putting FPGAs to Work in Software Radio Systems

Technology

FPGAs for Software Radio

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Figure 7

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 500 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

FPGAs Bridge the SDR Application Task Space

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.
Putting FPGAs to Work in Software Radio Systems

Evolving FPGA Generations

This table shows representative members from four generations of Xilinx devices currently used in Pentek Products: the Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-4.

The Virtex-E family includes a mix of configurable logic blocks, logic cells, system gates and block memory.

The Virtex-II family added built in hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing.

The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-II Pro is also the first family to incorporate RocketIO multigigabit serial transceivers to support the new switched gigabit serial fabrics.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 hardware multipliers for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.

Xilinx FPGAs in Pentek Products

The chart above shows a sampling of FPGAs and various Pentek hardware products that use them.

Each hardware product uses some of the FPGA resources to implement standard factory functions of the products such as interfaces, data formatting, state machines, and operating modes.

However, since many of the newer FPGAs are so large, even after all the standard factory functions have been implemented, a significant percentage of FPGA resources remain unused and available for customer use.

This chart shows the percentage of unused system gates and RAM available to the user for extending the FPGA to include custom algorithms. To address this requirement, Pentek has developed the GateFlow FPGA Design Resources.
Pentek's GateFlow Design Resources offer three ways to take advantage of these FPGA products.

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

If you need off the shelf algorithms for high-performance software radio functions you can take advantage of the GateFlow IP Core Library.

The third strategy is our GateFlow Factory Installed Cores, available as product options for many FPGA-based software radio products.

Let's start with the GateFlow FPGA Design Kit.

If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, data tagging.

These are also fully supported with our ReadyFlow® libraries and device drivers.

We also include a special User Block, positioned right in the data stream, so you can easily drop in your own custom signal processing algorithms.
Here's a simplified block diagram of a typical software radio module showing the FPGA as the large green box and external hardware devices connected to it.

The yellow blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces.

The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control, and clocks.

In the standard product, the User Block is configured as a straight wire between input and output.

If you, the FPGA designer, can create an IP core or a custom algorithm inside the User Block so that it conforms to the pin definition, you will have a very low-risk experience in recompiling and installing the custom code.

And remember, you can also make changes outside the User Block, since we provide source code for all the modules.

The GateFlow Design Kit is intended to be used with the Xilinx ISE Foundation Tool Suite and customers should be trained and familiar with this tool and FPGA design principles, in general.

The design kit installs as a complete project file within the ISE environment and includes all the project files that Pentek engineers used to create the standard factory product. These include configuration and definition files, VHDL source, JTAG definition files and I/O block diagrams.

The design kit also includes several utilities, but one important resource is the FPGA Loader Utility.
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GateFlow Design Kit Loader Utility

- FPGA Loader Utility
  - FPGA configuration loader utility executes on host or baseboard processor
  - Supports easy FPGA reconfiguration during runtime for adaptive processing
  - Supports easy FPGA reconfiguration for field upgrades
  - Eliminates need to disassemble system to modify hardware
  - Extends product longevity

Figure 15

GateFlow IP Core Library

- Pentek is a Xilinx AllianceCore member
- IP Cores are designed expressly for Xilinx FPGAs
- IP Cores are tested and certified for Pentek products
- The IP Core Library is compatible with the GateFlow Design Kit

Figure 16

Normally, the FPGA is loaded from a nonvolatile EEPROM with the standard factory configuration code, when the product is powered up.

The FPGA Loader Utility allows the processor associated with the FPGA product to reconfigure the FPGA as a software task, effectively overwriting the factory configuration code.

This can be done without turning off power, without disassembling the board or system and without attaching any special cables or harnesses to the board.

In this way, the FPGA can be reconfigured during initialization to install custom operational modes and features. It can also facilitate product upgrades and enhancements to dramatically extend product longevity.

The Loader Utility is especially useful as a runtime resource. The user can select a new mode of operation and cause a new FPGA configuration upload, to implement that mode as part of the runtime executable code.

Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

Pentek offers popular high-performance signal processing algorithms in the GateFlow IP Core Library. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products. The cores take full advantage of the numerous hardware multipliers to achieve highly-parallel processing structures that can dramatically outperform programmable RISC and DSP processors. They are fully compatible with the GateFlow FPGA Design Kit we just discussed.
This is a list of Model 4954 GateFlow IP Cores available from Pentek.

The first two are high-performance FFTs, followed by two wideband digital downconverters (DDCs).

Also included are a high-density 256-channel narrowband digital downconverter and a pulse compression core for radar.

Let’s start with the FFT core.

Dozens of FFT IP cores are available but here are two examples of 1k and 4k complex FFTs that have been optimized for speed.

Calculation time is proportional to clock speed and the maximum clock depends on the speed grade of the FPGA devices.

For these cores, the -6 device can be operated up to 140 MHz.

But at a reference clock frequency of 100 MHz, the core 404 executes a 4k complex FFT in just over 10 µsec.

How does that compare with a general purpose DSP or RISC processor? In fact, a 500 MHz G4 PowerPC takes ten times longer and a 300 MHz TI C6203 takes 20 times longer.

The message here is that if you need to do a fast FFT, strongly consider doing it in an FPGA.
Putting FPGAs to Work in Software Radio Systems

**Resources**

### Pipelined FFT Dataflow, IP Cores 401 and 402

- Cores 401 & 404 use QUAD pipelined architecture
- Four input & output streams staggered at 25% offset
  - Four input/output points for each input clock
- FFT calculation time for Core 404 (4096 points)
  - Four FFTs are computed in parallel every 4096 clocks
  - Effective Calculation time for each FFT = 4096 clocks / 4 = 1024 clocks
  - 100 MHz Clock Example: 4k FFT Time = 1024 x 10 ns = 10.24 usec

**Figure 19**

Here’s a simplified view of the dataflow into and out of the four stage FFT engine for the 4k point FFT.

Four separate input streams are processed in parallel with a 25% offset between the streams.

This explains why the effective FFT calculation time for the engine is 25% of the data collection time.

This core supports one channel with 75% input overlap processing, two channels with 50% input overlap processing or four independent channels with no overlap.

### Wideband DDC, IP Core 421

- Operates at input clock rates to 160 MHz
- Real or complex output, spectrum inversion & offset
- Requires XC2V1500 Xilinx Virtex-II FPGA (or larger)
- Two will fit inside the XC2V3000

**Figure 20**

This wideband digital downconverter uses a classic architecture of mixer, local oscillator and filter that takes full advantage of the hardware multipliers and memory inside the Virtex-II devices.

It offers real or complex inputs and outputs in several formats, six decimation settings from 2 to 64 and four sets of user loadable FIR coefficients for each setting.

It operates at a maximum frequency of 160 MHz.

Unfortunately, it won’t work for A/D converters operating at higher frequencies, like the AD9430 12-bit 215 MHz A/D converter.

So, how do we solve that problem?
By taking advantage of the ability to build parallel hardware structures in FPGAs, we can split the single input stream from the A/D into two simultaneous processing chains.

At the front end of the Core 422 wideband DDC, a demultiplexer sends even samples to the upper DDC arm and odd samples to the lower DDC arm.

A final stage combines the two decimated DDC streams into a single output.

This way, a 296 MHz input sample stream can be handled with two 148 MHz DDC cores operating in parallel.

What about performance of this core compared with an ASIC device?

Compared with the industry standard ASIC equivalent, the 421 and 422 Cores deliver higher sample rates, programmable filter coefficients and much better overall signal to noise performance because of improved bit accuracies in each stage.

In fact, four user selectable sets of FIR filter coefficients are available for each of the six decimation settings. These 24 sets of coefficients are stored in RAM structures within the FPGA. Users can enter new coefficient values during runtime without the need to recompile the FPGA.
Pulse Compression, IP Core 440

- Operates at input data rates up to 150 MHz
- 24 User Configurable Architectures
  - 16, 20, or 24 bit Resolution
  - 4k, 8k, and 16k Maximum FFT Sizes
  - Minimum Resource or Maximum Speed Configurations
- Block Floating Point arithmetic preserves dynamic range

This radar pulse compression core implements the required signal processing blocks for a radar receiver.

A reference pulse spectrum is stored in the Reference Spectrum RAM followed by a complex conjugate function. Input return echo pulses are processed by an FFT.

A complex multiplier multiplies the FFT output vector by the reference spectrum vector. An inverse FFT restores the signal to the time domain and produces the compressed output pulse.

Each stage uses adaptive block floating point scaling to maintain maximum dynamic range for each rank of the calculation.

Now let’s see what this core does in operation.

An outgoing radar pulse returns after time T1 from a closer target and after a longer time T2 from a more distant target.

The two return radar “chirps” are signals shown separately above but are actually combined in the feed from the radar horn. After processing with the pulse compression core, the two spikes shown below clearly show each target.
The GateFlow IP Core 430 is a 256-channel narrowband digital downconverter (DDC) designed for Xilinx Virtex-II Pro and Virtex-4 FPGAs.

Utilizing a unique architecture, this core achieves a very high channel-count-to-FPGA resource ratio. It provides up to 256 narrowband channels in one mid-sized FPGA. Each channel has completely independent 32-bit resolution programmable tuning and filter characteristics comparable to many conventional ASIC DDCs.

Within the core, the channelizer stage first splits the single wideband sampled input data stream into 1024 equally spaced frequency bands. Unlike traditional channelizers, each band significantly overlaps the adjacent band in frequency.

Using coarse tuning frequency information, the crossbar channel switch individually selects the most appropriate frequency band for each of the 256 channels.

An FIR compensation filter flattens the passband response of the selected band for delivery to a conventional DDC stage. This stage performs fine tuning of the desired output band across the flat portion of the input band. All 256 identical DDC channels then deliver independently tuned and decimated data through gain stages to the output multiplier.

Decimation is programmable from 1024 to 9984 in steps of 256, but must be the same for all 256 channels. For an input sample rate of 185 MHz, this results in usable output bandwidths from about 8 kHz to 80 kHz, covering a wide range of narrowband applications.

Filter coefficients for the DDC decimating filters are programmable to provide custom filtering characteristics. Overall rejection of adjacent channel signals is 75 dB.

The Core 430 can be installed within a single Virtex-II Pro VP50 and operates at input sample rates up to 180 MHz.
Factory Installed IP Cores

- Popular signal processing functions
- Standard off-the-shelf "hardware"
- Optimized for specific mezzanine cards
- Optimized for efficient FPGA resource utilization
- Optimized for execution & throughput speed
- Eliminates need for FPGA development
- Specified as an option to standard products
- No licensing or NDA Required
- Pentek ReadyFlow Board Support Libraries

The third GateFlow offering is the family of GateFlow Factory Installed IP Cores.

Pentek will install selected IP cores from the GateFlow IP Core Library on Pentek catalog products. Ordering an installed core is done by simply appending an option number to the model number.

All installed cores are fully tested and supported with Pentek ReadyFlow Board Support Libraries.

These installed cores allow customers to take advantage of these “turbocharged” products without investing in FPGA design skills and resources.

Installed Dual Wideband DDC, IP Core 421

- High Performance Dual Channel DDC
  - Takes full advantage of 14-bit A/D Converters
  - downloadable FIR filter coefficients
  - Precision local oscillator
  - Improved dynamic range

New 14-bit 105 MHz A/D converters are now available for many software radio applications. Pentek’s Core 421 Precision Wideband DDC, is an especially effective alternative to the popular GC1012B wideband ASIC that accepts only 12-bit A/D inputs.

Four sets of user programmable FIR filter coefficients for each of the six decimation settings, support signal processing filters with custom phase and frequency response characteristics.
For many signal intelligence and radar applications, the FFT is an extremely popular algorithm.

The Pentek Core 404 4k Complex FFT IP core can be installed in a two channel A/D module.

FFT features include input source selection of the A/D converter or the output of the wideband DDC ASIC, optional Hanning window, and an optional power calculation stage at the output.

The 215 MHz A/D converter featured in the Pentek Models 6821 and 6822 VXS A/D Converter VME boards can accommodate two Core 422 Extended Wideband DDC IP Cores.

The two Xilinx XC2VP50 devices are configured as two independently controlled digital downconverters. They offer a tuning range from DC to 107.5 MHz and output bandwidths as high as 86 MHz.
The Model 7140 PMC module accommodates the 256-Channel Digital Downconverter IP Core 430 within the VP50 FPGA. It provides an extremely high density digital receiver function. With two of these modules mounted on a 6U carrier board for VME or CompactPCI, each chassis slot can provide an unprecedented 512 channels of independently tuned narrowband DDCs.

Input data for the 430 core can be sourced from either of the two A/D converters. Output data is multiplexed to the PCI interface using the four FIFO buffers normally assigned to the four channels of the GC4016 DDC chip.

Tuning and control is provided across the PCI bus and is fully supported with ReadyFlow libraries and device drivers for Windows, VxWorks and Linux.

All standard factory functions of the Model 7140 have been preserved so that its GC4016 quad DDC can still be used. Data from the A/D converters can still be sent directly to the PCI interface.

In summary, the GateFlow FPGA Design Resources offer three ways to extend the functions of FPGAs.

The GateFlow FPGA Design Kit allows customers to add their own algorithms to Pentek catalog products.

The GateFlow IP Core Libraries are high-performance DSP algorithms designed expressly for Xilinx FPGAs and Pentek hardware products.

The GateFlow Factory Installed Cores allow customers to add powerful FPGA resources to Pentek board-level products easily and with full software library support.
# Pentek FPGA-Based Software Radio Product Summary

<table>
<thead>
<tr>
<th>Pentek Model</th>
<th>Type</th>
<th>Form</th>
<th>Input</th>
<th>Output</th>
<th>Number of DDC Channels</th>
<th>Number of FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>6230</td>
<td>NB</td>
<td>VIM-4</td>
<td>Ana</td>
<td>VIM</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>6231</td>
<td>NB</td>
<td>VIM-2</td>
<td>Ana</td>
<td>VIM</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>6232</td>
<td>NB</td>
<td>VIM-4</td>
<td>Dig</td>
<td>VIM</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>6235</td>
<td>WB</td>
<td>VIM-2</td>
<td>Ana</td>
<td>VIM</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>6236</td>
<td>WB</td>
<td>VIM-2</td>
<td>Ana</td>
<td>VIM</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>6250</td>
<td>MB</td>
<td>VIM-2</td>
<td>FPDP</td>
<td>VIM</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>6251</td>
<td>MB</td>
<td>VIM-2</td>
<td>FPDP</td>
<td>VIM</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>6822</td>
<td>MB</td>
<td>VME</td>
<td>Ana</td>
<td>FPDP</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>6823</td>
<td>MB</td>
<td>VME</td>
<td>Ana</td>
<td>FPDP</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>7131</td>
<td>MB</td>
<td>PMC</td>
<td>Ana</td>
<td>PCI</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>7140</td>
<td>MB</td>
<td>PMC</td>
<td>Ana</td>
<td>PCI</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>7142</td>
<td>MB</td>
<td>PMC</td>
<td>Ana</td>
<td>PCI</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7231</td>
<td>MB</td>
<td>cPCI</td>
<td>Ana</td>
<td>PCI</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>7240</td>
<td>MB</td>
<td>cPCI</td>
<td>Ana</td>
<td>PCI</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>7242</td>
<td>MB</td>
<td>cPCI</td>
<td>Ana</td>
<td>PCI</td>
<td>1/2</td>
<td>1/2</td>
</tr>
<tr>
<td>7631A</td>
<td>MB</td>
<td>PCI</td>
<td>Ana</td>
<td>PCI</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>7640</td>
<td>MB</td>
<td>PCI</td>
<td>Ana</td>
<td>PCI</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>7642</td>
<td>MB</td>
<td>PCI</td>
<td>Ana</td>
<td>PCI</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>


The above chart shows a partial listing of recent Pentek software radio products containing user programmable FPGA resources.

The center section shows the number of channels of each type of digital downconverter used in each product. The GateFlow IP Cores 421, 422 and 430 shown are available as factory installed options in certain products.

The right section of the chart shows the type and number of FPGAs used in each product. The largest device available is shown at the top of the column but smaller members of the same family are optionally available.

For the latest complete list and full specifications of all digital receiver products, be sure to visit online Pentek’s Software Radio Central: pentek.com/sftradcentral

For the latest listings and descriptions of Pentek’s GateFlow IP cores, be sure to visit FPGA Resources online at: pentek.com/gateflow
Putting FPGAs to Work in Software Radio Systems

Products

Dual Channel A/D and Wideband Receiver with FPGA - VIM-2

The Model 6235 Dual Channel Wideband Receiver in Figure 35 is primarily intended for digitizing wideband IF input signals. Each RF input is transformer-coupled to the A/D converter to support input signals up to 150 MHz for undersampling applications.

Two AD9432 A/D converters digitize the RF inputs to 12-bit samples. The sampling clock is derived from an internal 100 MHz crystal oscillator, an external front panel reference input or from an LVDS front panel ribbon cable clock and sync board that can be used to synchronize multiple 6235’s. As many as 80 Model 6235’s can be synchronized with Pentek’s Model 9190 Clock and Sync Generator to support systems with many channels.

The A/D digital outputs feed two TI/Graychip GC1012B wideband DDCs, capable of accepting data at the 100 MHz rate. These chips can be set for decimation values to support output bandwidths from 1.25 MHz to 40 MHz.

Both A/D outputs and both wideband DDC outputs are delivered into a Xilinx Virtex-II Series FPGA. Here, factory default logic allows channel selection, triggering, DDC bypass, and data packing modes.

FPGA densities range from 1 to 3 million gates (XC2V1000 or 3000) and an optional GateFlow FPGA Design Kit is available to support user-defined custom algorithms.

For applications requiring FFTs, two different installed FFT cores are available for either 1k- or 4k-point block sizes (Cores 401 and 404).
The Model 6236 is identical to the popular 6235 but incorporates two new 105 MHz 14-bit A/D Converters (Analog Devices AD6645-105). These converters offer two additional bits of resolution for improved accuracy and dynamic range over the 6235.

In addition to the GateFlow FPGA Design Kit, Pentek offers several popular GateFlow IP Cores as factory installed options for both the Model 6235 and Model 6236.

Because the TI/GC1012B wideband DDCs accept only 12-bit inputs, two of the A/D converter bits remain unused.

To take advantage of the additional A/D resolution, Pentek’s GateFlow Wideband DDC IP Core 421 can be factory installed in the FPGA. The core supports a full 16-bit input, improved dynamic range, and user-configurable FIR filter coefficients. For this reason, the GC1012B chips are offered as an option to save cost.

A complete radar pulse compression Core 440 has also been developed specially for the 6235 and 6236.

See page 15 for more information on factory installed IP Cores and visit the GateFlow Resources website for all the latest information: pentek.com/gateflow.
The Model 6250 Dual FPDP Adapter in Figure 37 supports very high-performance custom signal processing functions by incorporating two high-density FPGAs.

Two bidirectional FPDP ports transfer 32-bit data at clock rates up to 40 MHz. Support for FPDP-II ports allows clock rates as high as 100 MHz (400 MB/sec.)

The FPDP inputs are connected to two Xilinx Virtex-II FPGAs with densities of either 1 or 3 million gates each (XC2V1000 or 3000). The FPGAs are clocked from an on-board 100 MHz crystal oscillator. Factory default FPGA configuration code includes the FPDP interface and the VIM interface so standard units can be used as fast FPDP adapters.

Custom FPGA configuration code can be developed using the optional GateFlow FPGA Design Kit containing the VHDL source for the factory default configuration and provisions for adding user-defined algorithms. Each FPGA is equipped with two 64k x 16 SRAMs for storing data or coefficients, creating a more powerful environment for custom FPGA applications and incorporation of third party IP cores.

Pentek’s family of 68xx A/D converters deliver sampling rates from 215 MHz to 2 GHz and feature FPDP outputs completely compatible with the Model 6250. Since the 6250 can also transmit FPDP data, it can be connected to many other Pentek products including digital receivers, A/Ds and DSP boards.
The Model 6228 Dual Channel Wideband Digital Upconverter in Figure 38, uses two Texas Instruments DAC5686 digital upconverter chips that include an interpolation filter, a local oscillator, a complex mixer and two 16-bit D/A converters.

When operated as a digital upconverter, the maximum clock rate is 320 MHz. This allows digital baseband complex input sampling rates up to 80 MHz and output IF frequencies tunable up to 160 MHz.

For the real IF output mode, only one of the 16-bit D/A converters of each DAC5686 is used. For the complex output mode, both D/A converters are used to deliver both I and Q analog signals.

When operated in the D/A only mode, the frequency translation functions are not used. In this mode, the maximum clock frequency for the interpolation filter and D/A converters becomes 500 MHz. With two upconverter chips in the module, four independent data streams can be delivered to the four 16-bit D/A converters, with optional interpolation for generation of signal bandwidths as high as 200 MHz.

The Virtex-II FPGA can be used as a preprocessor front end for the upconverters to implement additional interpolation filtering or other custom signal processing functions. An arbitrary waveform generator could be constructed using internal FPGA memory for waveform storage. A complete GateFlow FPGA Design Kit is available.
The Model 7131, a 16-Channel Multiband Receiver, is a PMC module. The 7131 PMC may be attached to a wide range of industry processor platforms equipped with PMC sites. The faceplate of a PMC module fits in a cutout on the front panel of the processor board and the PCI bus interface to the processor board is made through connectors at the rear of the module.

Versions of the 7131 are also available as PCI boards (7631A) and 6U or 3U CompactPCI boards (7231 or 7331). All three products have similar features.

Two 14-bit 105 MHz A/D Converters (Analog Devices AD6645) accept transformer-coupled RF inputs through two front panel SMA connectors. Both inputs are connected to four TI/GC4016 quad DDC chips, so that all 16 DDC channels can independently select either A/D.

Four parallel outputs from the four DDCs deliver data into the Virtex-II FPGA which can be either the XC2V1000 or XC2V3000. The outputs of the two A/D converters are also connected directly to the FPGA to support the DDC bypass path to the PCI bus and for direct processing of the wideband A/D signals by the FPGA.

The unit supports the channel combining mode of the 4016s such that two or four individual 2.5 MHz channels can be combined for output bandwidths of 5 MHz or 10 MHz, respectively.

The sampling clock can be sourced from an internal 100 MHz crystal oscillator or from an external clock supplied through an SMA connector or the LVDS clock/sync bus on the front panel. The LVDS bus allows multiple modules to be synchronized with the same sample clock, gating, triggering and frequency switching signals. Up to 80 modules can be synchronized with the Model 9190 Clock and Sync Generator. Custom interfaces can be implemented by using the 64 user-defined FPGA I/O pins on the P4 connector.

The FPGA is fully supported with the GateFlow FPGA Design Kit and GateFlow FPGA IP Core Library. Software drivers support VxWorks, Windows and Linux processor board operating systems.
The Model 6821 shown in Figure 40 is a 6U single slot board with the AD9430 12-bit 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be used in one or both of the FPGAs to perform this function. This core can be incorporated by the customer using the GateFlow FPGA Design Kit or ordered as a factory installed option. Visit pentek.com/gateflow for more information.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.
The Model 6822 shown in Figure 41 is a 6U single slot VME board with two AD9430 12-bit, 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from each A/D converter flows into a Xilinx Virtex-II Pro FPGA where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be used in each FPGA to perform this function. This core can be incorporated by the customer using the GateFlow FPGA Design Kit or ordered as a factory installed option. Visit pentek.com/gateflow for more information.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.
Putting FPGAs to Work in Software Radio Systems

**Quad 500 MHz, 8-bit A/D and FPGA-based Digital Receiver - VME**

The Model 6823 shown in Figure 42 is a 6U single slot VME board with two dual Atmel AT84AD004 500 MHz 8-bit A/D converters.

Capable of digitizing input signals at sampling rates up to 500 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is derived from an external sinusoidal source.

Data from each of the four A/D converters flows into one of four Xilinx Virtex-4 XC4VSX55 FPGAs where optional signal processing functions can be performed. As the largest FPGA in the SX family, the XC4VSX55 is rich in processing resources.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board. A very high-speed digital downconverter IP core for the Model 6823 is currently under development at Pentek.

The customer will be able to incorporate this core into the Model 6823 by using the GateFlow FPGA Design Kit, or order it as a factory installed option.

An input LVDS front panel 32-bit port is connected to the first FPGA of the FPGA chain, while a 32-bit FPDP or FPDP II front panel port connects to the last FPGA for moving data out of the FPGA. Both ports support data transfers of 320 MB/sec and higher.

This architecture supports channelized applications such as communication systems and data summation applications such as beamforming.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides control paths for runtime applications.
Putting FPGAs to Work in Software Radio Systems

The Model 6826 shown in Figure 43 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 or XC2VP100 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board. A very high-speed digital downconverter IP core for the Model 6826 is currently under development at Pentek.

The customer will be able to incorporate this core into the Model 6826 by using the GateFlow FPGA Design Kit, or order it as a factory installed option.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is also available in a single-channel version.
The Model 7140 PMC module combines both transmit and receive capability with a high-performance Virtex II-Pro FPGA and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O.

The front end of the module accepts two +4 dBm full-scale analog RF inputs and transformer couples them into two 14-bit A/D converters running at 105 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources.

These resources include a quad digital downconverter, a digital upconverter with dual D/A converters, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and status engine with data and programming interfaces to each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Because the FPGA controls the data flow within the module as well as providing signal processing, the module can be configured for many different functions. In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals, developed using Pentek’s GateFlow and ReadyFlow® development tools.

The module includes a TI/GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters.

Each channel in the downconverter can be set with an independent tuning frequency and bandwidth.
The upconverter translates a real or complex baseband signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through its two 16-bit D/A converters. The digital upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MHz.

Inputs to the downconverter can come from many sources, including the input A/D converters, the FPGA signal processing engines, the SDRAM delay memory, or data sources on the PCI bus. The built-in clock/sync bus supports multiple module synchronization as well as dual on-board oscillators for independent input and output clock rates. Furthermore, the Model 7140 offers the VITA 42 XMC interface. This allows it to transfer data through optional Serial RapidIO, PCI-Express, or other switched fabric interfaces, which provide a high-speed streaming data path that is independent of the PCI bus.

A clock/sync bus allows synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection among multiple 7140s. One board acts as a master, driving clock, sync and gate signals out to a front panel flat cable bus using LVDS differential signaling. The master alone can drive as many as seven slaves. By using a Pentek Model 9190 Clock and Sync Generator to drive the signals, as many as 80 modules can be configured to operate synchronously.

For more information on the Model 7140 Software Radio Transceiver, visit pentek.com/sftradcentral.

As shown in Figure 43, this module is also available in a variety of form factors including PCI (Model 7640), 3U cPCI (Model 7340), 6U cPCI (Model 7240 with twice the density of the other models) and a PMC conduction-cooled version (Model 7140-700). These models are also available with IP Core 430, a 256-channel narrowband receiver, installed, see page 17.
The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

The front end of the module accepts two +4 dBm full-scale analog RF inputs and transformer couples them into four 14-bit A/D converters running at 125 MHz. The digitized output signals pass to the first Virtex-4 FPGA for signal processing or routing to other module resources.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

The upconverter translates a real or complex signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through the 16-bit 500 MHz D/A converters.

Two 4x switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the new XMC connector with two 2.5 GB/sec data links to the carrier board.
The built-in clock/sync bus supports multiple module synchronization as well as dual on-board oscillators for independent input and output clock rates.

Furthermore, the Model 7142 offers the VITA 42 XMC interface. This allows it to transfer data through optional Serial RapidIO, PCI-Express, or other switched fabric interfaces, which provide a high-speed streaming data path that is independent of the PCI bus.

A clock/sync bus allows synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection among multiple 7142s. One board acts as a master, driving clock, sync and gate signals out to a front panel flat cable bus using LVDS differential signaling. The master alone can drive as many as seven slaves. By using a Pentek Model 9190 Clock and Sync Generator to drive the signals, as many as 80 modules can be configured to operate synchronously.

For more information on the Model 7140 Software Radio Transceiver, visit pentek.com/sfradcentral.

As shown in Figure 46, this module is also available in a variety of form factors including PCI (Model 7642), 3U cPCI (Model 7342), 6U cPCI (Model 7240, or Model 7240D with twice the density of the other models).
The Pentek RTS 2501 in Figure 48 is one of several highly-scalable, real-time recording systems for acquiring, downconverting, processing, and recording wideband signals.

The heart of the RTS 2501 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

Attached to the 4205 I/O Processor are two Model 6236 Dual Channel Wideband Receiver VIM modules, each with two 14-bit 105 MHz A/D converters, two TI/GC1012B wideband digital downconverters and a Virtex-II FPGA.

A built-in Fibre Channel interface connects directly to RAID or JBOD arrays for real time storage to 6 terabytes and higher, at rates up to 160 MB/sec. Standard RS-232 and 100 baseT Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from four to 80 channels in a single 6U VMEbus chassis, the RTS 2501 serves equally well as a real-time system for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on pentek.com.
Real-Time 215 MHz Recording System with FPGA Processing

The Pentek RTS 2503 in Figure 49 extends the range of highly-scalable, real-time recording systems for acquiring, downconverting, processing, and recording wideband signals to 215 MHz sampling frequency, by utilizing the single-channel Model 6821 or the dual channel Model 6822, 215 MHz 12-bit A/D converters. These attach to the Model 4205 I/O Processor with two Pentek Model 6226 FPDP Adapter VIM-2 modules. This system occupies two VMEbus slots.

Again, the heart of the RTS 2503 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

A built-in Fibre Channel interface connects directly to RAID or JBOD arrays for real time storage to 6 terabytes and higher, at rates up to 160 MB/sec. Standard RS-232 and 100 baseT Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from one to 20 channels in a single 6U VMEbus chassis, the RTS 2503 allows the design engineer to take advantage of the latest technology for research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on pentek.com.
Real-Time 105 MHz Recording System with Multiband Transceiver and FPGA Processing

The Pentek RTS 2504 in Figure 50 utilizes the Model 7140 Multiband Transceiver PMC/XMC module described on page 28. The Model 7140 combines downconverter and upconverter functions in one module and offers real-time recording and playback capabilities.

Again, the heart of the RTS 2504 is the Pentek Model 4205 I/O Processor featuring a 1 GHz MPC7457 G4 PowerPC, mezzanine sites for both VIM and PMC modules, and two Xilinx Virtex-II FPGAs. The G4 PowerPC acts both as an executive for managing data transfer tasks as well as performing digital signal processing or formatting functions.

A built-in Fibre Channel interface connects directly to RAID or JBOD arrays for real time storage to 6 terabytes and higher, at rates up to 160 MB/sec. Standard RS-232 and 100 baseT Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.

Scalable from 2 to 40 channels in a single 6U VMEbus chassis, the RTS 2504 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

More information on RTS systems on pentek.com.
Putting FPGAs to Work in Software Radio Systems

**Systems**

**DSP Boards for VMEbus**

- Freescale Altivec G4 PowerPC
- Texas Instruments C6000 DSPs
- Single, Dual, Quad and Octal Processor versions
- PMC, VIM, PCI and cPCI Mezzanines
- RACEway, RACE++, FPDP and Fibre Channel Interfaces

**Figure 51**

Pentek offers a comprehensive array of VMEbus DSP boards featuring the TMS320C6000 family of processor products from Texas Instruments and the Altivec G4 PowerPC from Freescale.

On-board processor densities range from one to eight DSPs with many different memory and interface options available.

The Model 4290/91/92/93 series of VIM quad processor boards features the Texas Instruments latest TMS320C6000 family of fixed and floating point DSPs that represent a 10-fold increase in processing power over previous designs.

The Models 4294 and 4295 VIM processor boards feature four MPC74xx G4 PowerPC processors utilizing the Altivec vector processor capable of delivering several GFLOPS of processing power.

The Model 4205 G4 PowerPC I/O processor board accepts both VIM and PMC mezzanines and includes built-in Fibre Channel and dual RACE++ interfaces.

Once again, the ability of the system designer to freely choose the most appropriate DSP processor for each software radio application, facilitates system requirement changes and performance upgrades.

Full software development tools are available for workstations running Windows, Solaris, and Linux with many different development system configurations available.

**Summary**

- Communications Algorithms
  - Digital down conversion, demodulation, dec
- Beam Forming
  - Direction finding, phased array processing,
- Analysis
  - FFTs, pulse compression, decryption, static
- High-Speed Interfaces
  - Switched serial fabric interfaces: Serial Rap
- Triggering and Gating
  - Radar acquisition and synchronization
- Memory Control
  - DMA engines, circular delay buffers, transis
- Formatting and Packing
  - Flexible data manipulation for special I/O, p

As we have seen, FPGAs are truly an integral part of the latest generation of software radio products.

Not only are they being used with traditional digital signal processing algorithms but also in the management of data acquisition, buffering, triggering and timing aspects of high-performance real time systems.

Pentek offers not only a wide range of hardware products featuring the latest FPGAs, but also the FPGA development resources and knowledgeable applications engineers to help you get the most out of these products.

We encourage you to contact your Pentek sales engineers today to discuss your system needs.

And be sure to visit our extensive web site for the latest product and technical information: www.pentek.com
Putting FPGAs to Work in Software Radio Systems

The following live links provide you with additional information about the Pentek Products and Systems presented in this handbook. Live links are also provided to other handbooks or brochures that may be of interest in your software radio development projects.

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### Handbooks & Brochures

- [Click here](#) Digital Receiver Handbook: Basics of Software Radio
- [Click here](#) Critical Techniques for High-Speed A/D Converters in Real-Time Systems
- [Click here](#) High-Speed A/D Boards & Real-Time Systems
- [Click here](#) Model 4205 PowerPC Processor Board