

16AI64

64-Channel, 16-Bit Analog Input PMC Board With 500 KSPS Input Conversion Rate

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

PMC-16AI64:	PMC , Single-width
PCI-16AI64:	PCI , short length
cPCI-16AI64:	cPCI , 3U
PC104P-16AI64:	PC104-Plus
PCIe-16AI64:	PCI Express
PCIe104-16AI64:	PCIe , one-lane on PC/104 form factor

See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

Features Include:

- 64 Single-ended or 32 Differential 16-Bit Scanned Analog Input Channels
- Conversion Rates to 500K Conversions-per-Second in Single-Channel Mode
- Scan Rates to 350K Channels-per-Second in Multichannel Scanning Mode
- Input Ranges Selectable as $\pm 10V$, $\pm 5V$ or $\pm 2.5V$
- Data is Buffered through a 64K-sample FIFO
- Optional Low-Latency configuration replaces the FIFO buffer with 64 discrete data registers
- Continuous and Burst (One-Shot) Input Modes
- Sync Input/Output (Alternate Function for Channels 62,63)
- Scan Sizes from Two to 64 Channels-per-Scan; or Single-Channel sampling of any Channel
- Internal Rate Generator Implements a 32-Bit Divider
- Internal Autocalibration upon command
- DMA Engine Minimizes Host I/O Overhead
- Each Input Channel Buffered for Minimum Crosstalk and Input Bias Current
- Completely Software-Configurable; No Field Jumpers
- Single-width PMC Form Factor with EMI Shield and Panel Bezel

Applications Include:

- | | | |
|----------------------------|-----------------------|------------------------------|
| ✓ Acoustics Analysis | ✓ Voltage Measurement | ✓ Automatic Test Equipment |
| ✓ Analog Inputs | ✓ Process Monitoring | ✓ Audio Waveform Analysis |
| ✓ Data Acquisition Systems | ✓ Industrial Robotics | ✓ Environmental Test Systems |

Functional Description:

The PMC-16AI64 board is a scanning analog digitizer that performs high-speed sampling and 16-bit A/D conversion of as many as 64 single-ended or 32 differential analog input channels. The resulting 16-bit sampled data is available to the PCI bus through a 64K-Sample FIFO buffer. An optional Low-Latency option is available in which the FIFO buffer is replaced with 64 contiguous discrete data registers that are updated continuously. All operational parameters are software configurable.

The analog inputs can be sampled in scans of 4, 8, 16, 32 or 64 single-ended channels, or in scans of 4, 8, 16 or 32 differential channels. The scan rate can be controlled internally up to 175,000 scans per second for a 2-channel scan, or any single channel can be sampled at 500,000 samples per second. A Sync input/output signal can replace Channels 62,63 to permit multiple boards to perform synchronous scanning. All inputs are buffered to avoid the high cross talk and input bias currents common with nonbuffered multiplexers.

The internal auto calibration utility uses hardware D/A converters to correct for offset and gain errors in the input signal path, and eliminates the missing codes that are inevitably introduced when software correction methods are used. A selftest switching network routes calibration signals through the input multiplexer to the A/D converter to support internal auto calibration, and permits board integrity to be verified by the host. Auto calibration is performed automatically after reset or upon demand from the PCI bus, and calibrates the offset and gain of the converter to a precision internal reference voltage.

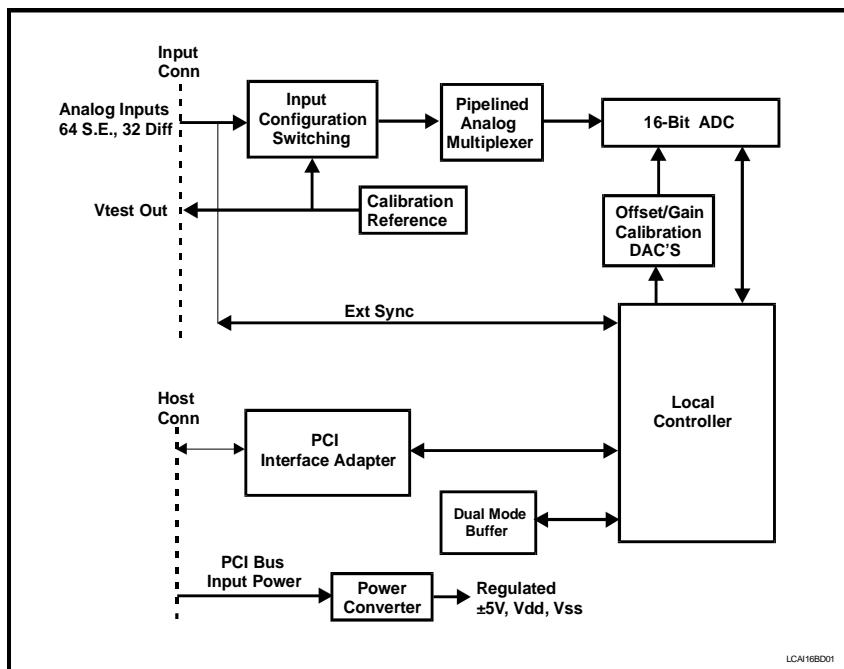


Figure 1. PMC-16AI64; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density 68-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

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ELECTRICAL SPECIFICATIONS

At +25 °C, with specified operating voltages

Input Characteristics:

Configuration:	64 single-ended or 32 differential analog input channels
Voltage Ranges:	Software configurable as ±10 Volts, ±5 Volts or ±2.5 Volts; or optionally factory configured for a fixed range of ±10 Volts, ±5 Volts or ±2.5 Volts
Input Impedance:	1.0 Megohm typical.
Common Mode Rejection:	60 dB typical, DC-60 Hz (Differential inputs)
Common Mode Range:	Same as selected voltage range, with zero normal mode signal (Diff inputs)
Bias Current:	Less than 80 nanoamps
Crosstalk Rejection:	85dB in single-channel mode, 80dB in scanning mode, typical, DC-10kHz
Overvoltage Protection:	±30 Volts with power applied*; ±15 Volts with power removed.

* Inputs 62,63 (Alternate function TTL Sync I/O) limited to -0.5 to +7.0 Volts

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Maximum Sample Rate:	Single-Channel Mode:	500K conversions per second	
	Multichannel (Scan) Mode:	350K conversions per second	
Maximum Scan Rate:	Single-Channel Mode:	500K conversions per second	
	Multichannel (Scan) Mode:	350K divided by number of channels in scan	
Channels per scan:	2, 4, 8, 16, 32 or 64 Single-ended channels; 2, 4, 8, 16 or 32 differential channels. Or, any single channel.		
DC Accuracy: (Maximum composite error after autocalibration)	<u>Range</u>	<u>Midscale Accuracy</u>	<u>Fullscale Accuracy</u>
	±10V	± 3mv	± 4mv
	±5V	± 2mv	± 3mv
	±2.5V	± 1mv	± 2mv
Integral Nonlinearity:	±0.007 percent of FSR, typical		
Differential Nonlinearity:	±0.003 percent of FSR, maximum		

Analog Input Operating Modes and Controls:

Input Data Buffer:	64K-sample FIFO, or optional Low-Latency configuration with 64 discrete data registers.	
Analog Input Modes:	Continuous Scan:	Analog inputs are scanned continuously.
	Burst Scan:	Each scan is initiated either by the internal rate generator, or by a hardware TTL input or a software sync input
	Single Channel:	Any single selected channel is sampled continuously
	Selftest:	Autocalibration and Selftest modes

Analog Input Operating Modes and Controls (Continued):

Rate Generator: Programmable from 0.01 - 500,000 conversions per second. External triggering is available through Channel 62,63 pins.

Input Data Format: Selectable as offset binary or as two's complement

PCI Interface:

Conforms to PCI Specification 2.3, D32, 33MHz, 5V signaling.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

□ Power Requirements

+5VDC ±0.2 VDC at 1.0 Amp, maximum

Maximum Power Dissipation: 4.5 Watts, Side 1
 0.8 Watt, Side 2

□ Physical Characteristics (PMC Form Factor)

Height: 13.5 mm (0.53 in)

Depth: 149.0 mm (5.87 in)

Width: 74.0 mm (2.91 in)

Shield: Side 1 can be protected by an optional EMI shield.

□ Environmental Specifications

Ambient Temperature Range: Operating: 0 to +65 degrees Celsius inlet air
 Storage: -40 to +85 degrees Celsius

Relative Humidity: Operating: 0 to 80%, non-condensing
 Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

Cooling: Conventional convection cooling; 150 LFPM

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A -B -C", as indicated below. For example, model number PMC-16AI64-2-FB describes a board with 64 input channels and the standard FIFO data buffer with standard System I/O connector.

Basic Model Number	Form Factor
PMC-16AI64	PMC (Native)
PCI-16AI64¹	PCI, short length
cPCI-16AI64¹	cPCI, 3U
PCIe-16AI64¹	cPCI, 3U
PC104P-16AI64	PC104-Plus
PCIe104-16AI64^{1,2}	PCIe, one-lane on PC/104 form factor

¹ Module installed and tested on an adapter, with mechanical and functional equivalency.
Contact factory for availability in native form factors.

² PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	32 Channels	A = 1
	64 Channels	A = 2
Data Configuration	FIFO Buffer	B = FB or Blank
	Low Latency	B = LL
System I/O Connector	68 Pin RN P50 68 Pin SCSI 3	C = Blank C = SCSI3

STANDARD SYSTEM I/O CONNECTIONS

Table 1. System I/O Connector Pin Functions

ROW-A			ROW-B		
PIN	SIGNAL		PIN	SIGNAL	
	S.E. MODE	DIFF MODE		S.E. MODE	DIFF MODE
1	INP00	INP00 HI	1	INP32	INP16 HI
2	INP01	INP00 LO	2	INP33	INP16 LO
3	INP02	INP01 HI	3	INP34	INP17 HI
4	INP03	INP01 LO	4	INP35	INP17 LO
5	INP04	INP02 HI	5	INP36	INP18 HI
6	INP05	INP02 LO	6	INP37	INP18 LO
7	INP06	INP03 HI	7	INP38	INP19 HI
8	INP07	INP03 LO	8	INP39	INP19 LO
9	INP08	INP04 HI	9	INP40	INP20 HI
10	INP09	INP04 LO	10	INP41	INP20 LO
11	INP10	INP05 HI	11	INP42	INP21 HI
12	INP11	INP05 LO	12	INP43	INP21 LO
13	INP12	INP06 HI	13	INP44	INP22 HI
14	INP13	INP06 LO	14	INP45	INP22 LO
15	INP14	INP07 HI	15	INP46	INP23 HI
16	INP15	INP07 LO	16	INP47	INP23 LO
17	AGND	AGND	17	AGND	AGND
18	AGND	AGND	18	AGND	AGND
19	INP16	INP08 HI	19	INP48	INP24 HI
20	INP17	INP08 LO	20	INP49	INP24 LO
21	INP18	INP09 HI	21	INP50	INP25 HI
22	INP19	INP09 LO	22	INP51	INP25 LO
23	INP20	INP10 HI	23	INP52	INP26 HI
24	INP21	INP10 LO	24	INP53	INP26 LO
25	INP22	INP11 HI	25	INP54	INP27 HI
26	INP23	INP11 LO	26	INP55	INP27 LO
27	INP24	INP12 HI	27	INP56	INP28 HI
28	INP25	INP12 LO	28	INP57	INP28 LO
29	INP26	INP13 HI	29	INP58	INP29 HI
30	INP27	INP13 LO	30	INP59	INP29 LO
31	INP28	INP14 HI	31	INP60	INP30 HI
32	INP29	INP14 LO	32	INP61	INP30 LO
33	INP30	INP15 HI	33	INP62/ SYNC HI *	INP31 HI/ SYNC HI *
34	INP31	INP15 LO	34	INP63/ SYNC LO*	INP31 LO/ SYNC LO*

* Software-selected.

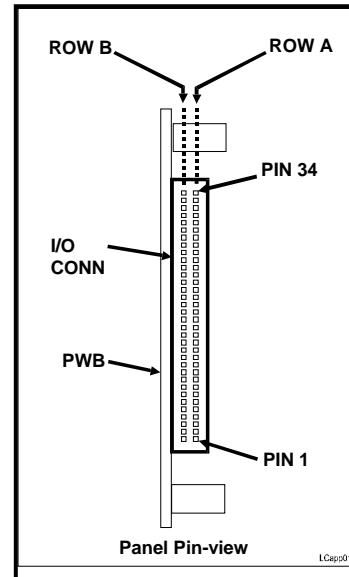


Figure 2. System Input Connector

System Mating Connector:

68-pin 0.050" Subminiature connector:

Robinson Nugent #P50-068-STG or equivalent.

Optional SCSI-3 SYSTEM I/O CONNECTIONS

Table 2. SCSI System I/O Connector Pin Functions

PIN	SIGNAL	
	S.E. MODE	DIFF MODE
1	INP00	INP00 HI
2	INP01	INP00 LO
3	INP02	INP01 HI
4	INP03	INP01 LO
5	INP04	INP02 HI
6	INP05	INP02 LO
7	INP06	INP03 HI
8	INP07	INP03 LO
9	INP08	INP04 HI
10	INP09	INP04 LO
11	INP10	INP05 HI
12	INP11	INP05 LO
13	INP12	INP06 HI
14	INP13	INP06 LO
15	INP14	INP07 HI
16	INP15	INP07 LO
17	AGND	AGND
18	AGND	AGND
19	INP16	INP08 HI
20	INP17	INP08 LO
21	INP18	INP09 HI
22	INP19	INP09 LO
23	INP20	INP10 HI
24	INP21	INP10 LO
25	INP22	INP11 HI
26	INP23	INP11 LO
27	INP24	INP12 HI
28	INP25	INP12 LO
29	INP26	INP13 HI
30	INP27	INP13 LO
31	INP28	INP14 HI
32	INP29	INP14 LO
33	INP30	INP15 HI
34	INP31	INP15 LO

PIN	SIGNAL	
	S.E. MODE	DIFF MODE
35	INP32	INP16 HI
36	INP33	INP16 LO
37	INP34	INP17 HI
38	INP35	INP17 LO
39	INP36	INP18 HI
40	INP37	INP18 LO
41	INP38	INP19 HI
42	INP39	INP19 LO
43	INP40	INP20 HI
44	INP41	INP20 LO
45	INP42	INP21 HI
46	INP43	INP21 LO
47	INP44	INP22 HI
48	INP45	INP22 LO
49	INP46	INP23 HI
50	INP47	INP23 LO
51	AGND	AGND
52	AGND	AGND
53	INP48	INP24 HI
54	INP49	INP24 LO
55	INP50	INP25 HI
56	INP51	INP25 LO
57	INP52	INP26 HI
58	INP53	INP26 LO
59	INP54	INP27 HI
60	INP55	INP27 LO
61	INP56	INP28 HI
62	INP57	INP28 LO
63	INP58	INP29 HI
64	INP59	INP29 LO
65	INP60	INP30 HI
66	INP61	INP30 LO
67	INP62/ SYNC HI *	INP31 HI/ SYNC HI*
68	INP63/ SYNC LO*	INP31 LO/ SYNC LO*

* Software-selected.

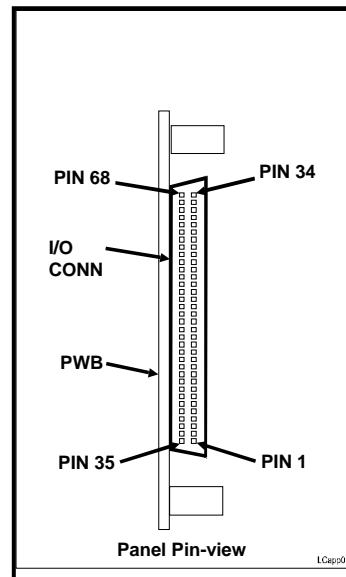


Figure 3. SCSI-3 System Input Connector

System Cable Mating Connector:

68-pin 0.050" Subminiature connector with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref):

Amp # 787170-7.

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