ADQ108

ADQ108 is a single channel high speed digitizer in the ADQ V6 Digitizer family. The ADQ108 has an outstanding combination of dynamic range and unique bandwidth, which enables demanding measurements such as RF/IF sampling of very wide band signals.

ADQ108 is optimized for dynamic performance over a wide bandwidth, which makes it ideal for broadband applications such as IF/RF sampling and high-speed data recording. The ADQ108 offers an easy-to-use API that allows easy integration into any application.

The ADQ108 is connected to the host PC with a USB3.0 interface for stand-alone operation or an eight-lane cPCIe interface for integration into the host PC. It is also available for modular instrumentation supporting cPCIe / PXIe and M-TCA.4 form factors.

ADQ108 Development Kit

The ADQ108 is equipped with an powerful Xilinx V6 LX240T FPGA which is partly available for customized real time applications.

SP Devices' ADQ108 Development Kit is an optional FPGA programming tool that enables custom real time signal processing of streaming data. More details about this product can be found in the datasheet for the ADQ Development Kit.

Ordering information

Table 1:

ORDERING INFORMATION	
Product	ADQ108
AVAILABLE OPTIONS	
USB 3.0	–USB
cPCIe / PXIe	–PXIE
PCIe	–PCIE
M-TCA.4	–MTCA
Positive DC-offset	–PB
Negative DC-offset	–NB
RELATED PRODUCTS	
ADQ108 Development Kit	ADQ108 Dev Kit

Features

- 7 / 6.4 / 6 GSPS sampling rate
- 8 bits resolution
- 2 GHz analog bandwidth
- Internal and external clock reference
- Clock reference output
- External trigger input and output
- Internal trigger
- Multi record >1 MHz PRF
- Time stamp
- 1 GSamples data memory
- Data interface USB3.0 / cPCIe / PXIe /PCIe / M-TCA.4
- FPGA available for customized applications

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

1 Technical data[1]

Table 2:

KEY PARAMETERS		
Number of channels	1	channels
Digitizer Resolution	8	bits
Sampling rate	7 / 6.4 / 6	GSPS
Data memory	1	GSample
Impedance AC	50	Ω
Bandwidth (–3 dB)	6 k – 2 G	Hz
Input voltage range	700	mV_{pp}
Connector	SMA	

Table 3:

ANALOG INPUT[1 2]			
ENOB	245 MHz	7.2	bits
	748 MHz	7.0	bits
	1.5GHz	6.8	bits
	3 GHz	6.2	bits
SFDR	245 MHz	60	dB
	748 MHz	58	dB
	1.5GHz	56	dB
	3 GHz	51	dB
SNR	245 MHz	46	dB
	748 MHz	45	dB
	1.5GHz	44	dB
	3 GHz	41	dB
THD	245 MHz	–58	dBc
	748 MHz	–57	dBc
	1.5GHz	–52	dBc
	3 GHz	–50	dBc

1. Constant input power, **Figure 2**
2. Time-interleaving spurs are excluded.

Table 4:

GPIO		
Number of GPIO	5	
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	Micro DSUB 9 way	

Table 5:

CLOCK REFERENCE OUTPUT		
Frequency	Set by clock reference	
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector M-TCA.4	MMCX	
Connector other formats	MCX	

Table 6:

EXTERNAL CLOCK SOURCE		
Frequency 4 channels mode	FS	MHz
Frequency 2 channels mode	FS/2	MHz
Signal level (min – max)	0 – 10	dBm
	0.64 – 2	Vpp
Impedance AC	50	Ω
Duty cycle	50%	
Connector	SMA	

Table 7:

CLOCK REFERENCE INPUT		
Internal clock reference		
Frequency	10	MHz
Accuracy	± 5 ± 0.5/y	ppm
External clock reference		
Frequency (min – max)	1 – 250	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector M-TCA.4	MMCX	
Connector other formats	MCX	
PXIe clock reference[1]		
PXIe clock	100	MHz
PXIe sync[2]	10	MHz

1. Available on PXIe form factor only
2. Jitter reduced by PXIe clock in digitizer

1. All values are typical unless otherwise noted.

Table 8:

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–0.4 to 2.4	V
Threshold rising/falling edge	500	mV
Sensitivity	200	mV
Jitter	25	ps
Resolution	2/FS	s
Pre-trigger buffer	Up to batch size	
Trigger hold off	2^{34} samples	
Multi record batch size	1 to entire memory	
Multi record max PRF	1.8 MHz	
Connector M-TCA.4	MMCX	
Connector other formats	MCX	

Table 9:

TRIGGER OUTPUT		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Connector M-TCA.4	MMCX	
Connector other formats	MCX	

Table 10:

POWER SUPPLY		
Supply Voltage	12	V
Power	30	W
Connector USB	Desk to power supply included.	
Connector PCIe	6-pin ATX power	
Connector cPCIe/PXIe	from slot	
Connector MTCA	from slot	

Table 11:

ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	

2 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

Table 12:

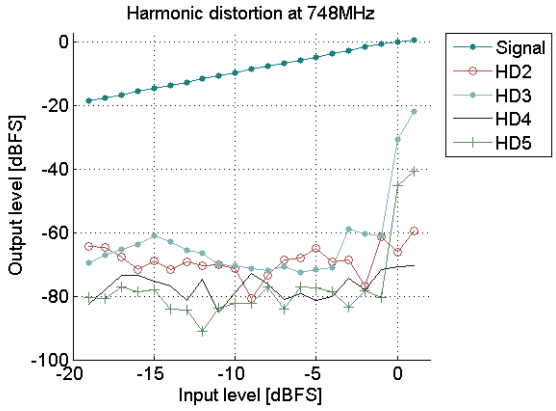
ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (sine wave < 2GHz)		750 mV_{RMS}
Analog input (sine wave >2GHz)		1.5 V_{RMS}
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 °C	45 °C

The ADQ108 has a built in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ108 from overheating by shutting down parts of the device.

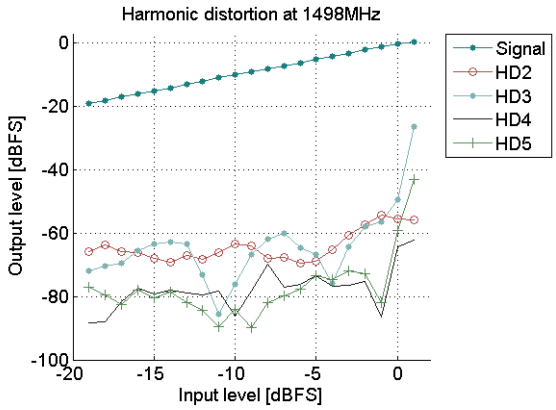
The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

3 Dynamic performance

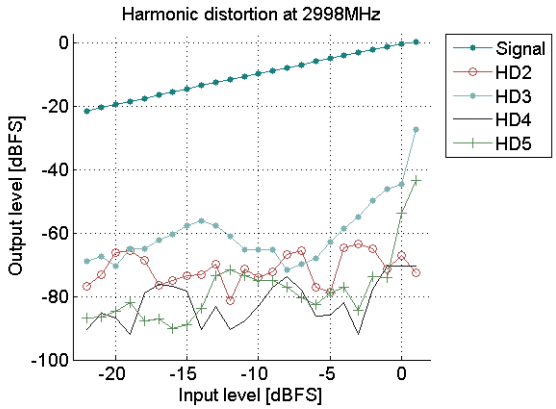
3.1 Linearity



(a) Input signal frequency 748 MHz



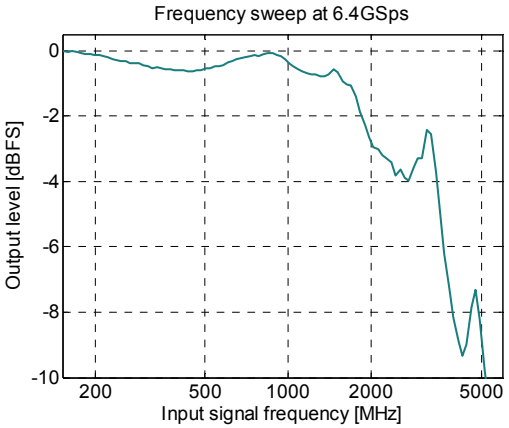
(c) Input signal frequency 1498 MHz



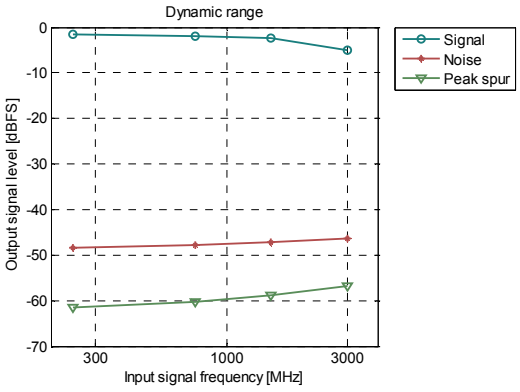
(c) Input signal frequency 2998 MHz

Figure 1: Harmonic distortion at different frequencies. Sampling rate 6.4 GSPS.

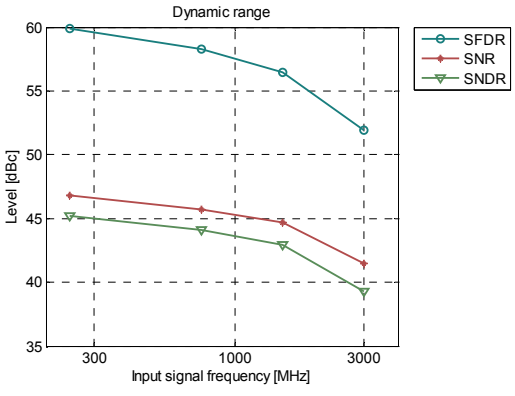
3.2 Frequency response



(a) Signal transfer function



(b) SNR and SFDR at constant input power. Excluding time-interleaving spurs.



(c) Dynamic range. Excluding time-interleaving spurs.

Figure 2: Input signal frequency sweep. Sampling rate 6.4 GSPS.

4 Architecture

4.1 Block diagram

The digitizer includes an analog front-end with signal conditioning and A/D conversions and a digital back-end for data flow control, triggering and host communication, see **Figure 3**.

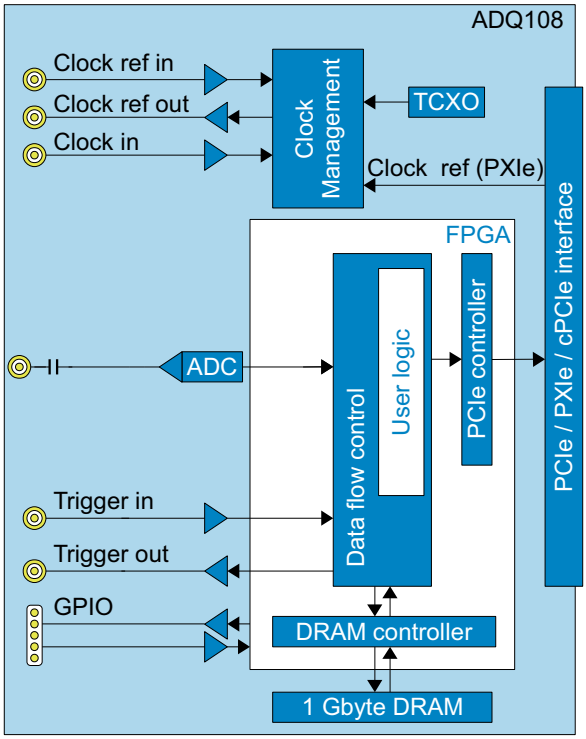


Figure 3: Block diagram 4 channels mode.

4.2 Analog front-end, AFE

The analog input is single-ended AC-coupled 50 Ohm. The vertical resolution of the ADC is 8 bits and it operates up to 7 GSPS.

4.3 Pre-biased DC-offset front-end options

For unipolar signals, a DC-offset is available in the front-end. It places the zero level at a pre-biased level and the entire signal range can be used to measure the pulses. This effectively doubles the dynamic range for unipolar pulses.

The DC-offset is installed in factory.

A positive DC-offset (for negative pulses) is available at 90% of the signal range. See

Order code: –PB

A negative DC-offset (for positive pulses) is available at 10% of the signal range.

Order code: –NB

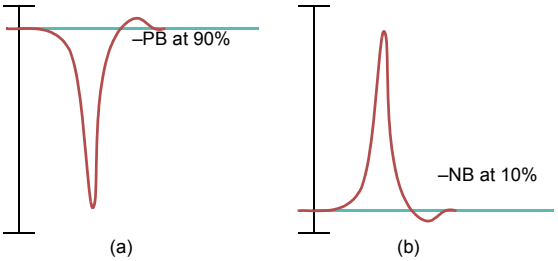


Figure 4: DC-offset options.

4.4 Data recording

There are several methods for data recording to serve different use cases;

- Multi-record recording in on-board DRAM for very long records.
- Level trigger for data driven capture
- Continuous multi-record via on-board DRAM for acquisition of long records during long measurement time.
- Continuous streaming of data to the host PC for real time analysis of data[1]

To support data recording, there is on board DRAM of 1 GBytes. The interface to the host PC enables up to 3.6 GBytes/s over a Gen2 x8 PCIe interface.

4.5 Trigger

There are several trigger modes;

- External for synchronization
- Level trigger for data driven acquisition
- Software for user's control
- Internal for automatic sequencing

There is also a trigger output for triggering external equipment. The trigger timing is controlled by pre-trigger buffer and trigger delay parameter settings.

1. This mode required ADQ108 Development Kit for data rate reduction.

4.6 GPIO

The ADQ108 is equipped with five bi-directional GPIOs. The GPIOs are controlled from software, but can also be accessed from the ADQ108 Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.

#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

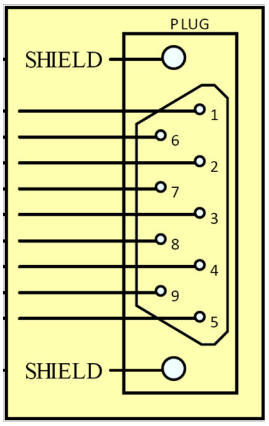


Figure 5: GPIO connector diagram.

5 Software tools

5.1 Operating systems

The software package includes drivers for the main operating systems.

Table 13:

OPERATING SYSTEM	
Windows 7	32 bit and 64 bit
Windows 8 / 8.1	
Windows 10	When available
Linux[1]	Kernel 2 and 3, 32 and 64 bits

1. Contact SP Devices sales representative for information about distributions.

5.2 ADCaptureLab

The ADQ108 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 6**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ108 operate as a desktop oscilloscope.

Please note that ADCaptureLab is available for Windows only.

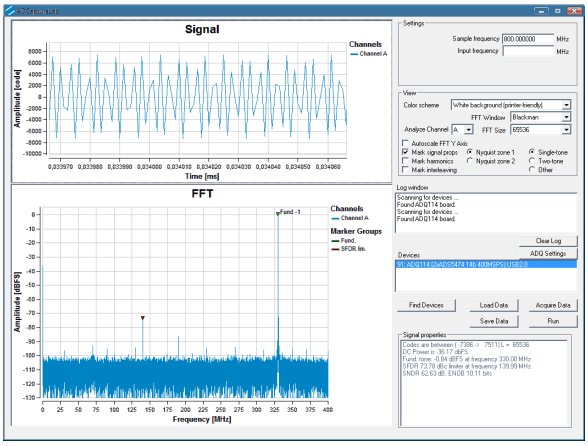


Figure 6: ADCaptureLab (Typical)

5.3 Software development kit (SDK)

The ADQ108 digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ108.

The SDK includes programming examples and reference projects for C/C++ and MATLAB. The ADQAPI users guide in detail describes all functions. Many examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

Table 14:

APPLICATION SOFTWARE	
ADCaptureLab[1]	Acquisition and analysis
MATLAB[1]	API, examples
C/C++	API, examples
.NET (C#, VB)	API, examples
Python	Example scripts
LabView	DLL import

1. Windows only

6 Host PC interface

The ADQ V6 digitizer family supports various number of interfaces. The digital interface is used for control and data transfer between the host and the digitizer.

6.1 Firmware upgrade interface

Regardless of the selected data interface, there is always an additional USB interface for firmware upgrade. This connection is not related to the data and control interface.

6.2 USB3.0 interface

With the USB interface, the digitizer is easily connected to any computer.

Table 15:

USB INTERFACE		
Standard	USB3.0	
Data rate sustained	200	MB/s
Box size	53 x 106 x 166	mm3

(a) Front panel

(b) Rear panel

Figure 7: ADQ108 stand alone box

Order code: –USB

6.3 CompactPCI Express / PXI Express

The ADQ108 is available in a form factor for modular instrumentation in a Compact PCI Express or PXI Express chassis.

Table 16:

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Sustained data rate[1]	3.2	GByte/s
PXIe card size	3U 2 slot 8TE	

1. This is depending on the capacity of the chassis and controller.

Figure 8: Typical cPCIe / PXIe card

Order code: –PXIE

6.4 PCI Express interface

The PCI Express interface is intended for integration in a PC.

Table 17:

PCIe INTERFACE		
Data rate	Gen2	
Bus width electrical	8	lanes
Sustained data rate[1]	3.2	GByte/s
Bus width mechanical[2]	16	lanes
Board height	2	slots
Board length (	167	mm

1. This is depending on the capacity of the PC
2. The wide contact is required to support the weight of the board.

Figure 9: ADQ108–PCIE card.

Order code: –PCIE

6.5 Micro-TCA interface

The ADQ V6 Digitizer family is available with digital back-end and interfaces for Micro-TCA.

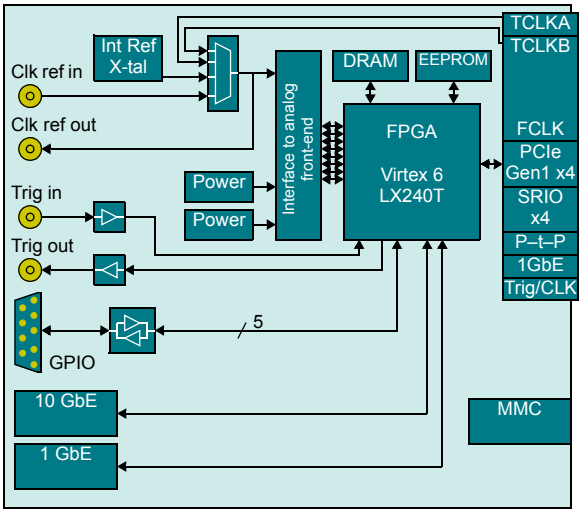


Figure 10: Block diagram of digital back-end for Micro-TCA.

Table 18:

MICRO-TCA BOARD SIZE	
Board width	Double width (~148.5mm)
Board height	Mid-size (~18mm)

Some of the pins in the backplane connector are used for the standard digitizer functions. Some are available for custom design using the ADQ108 Development Kit for custom implementations.

Table 19:

MICRO-TCA INTERFACE		
Signal	Port	Status
1GbE	0	ADQ108 Dev Kit
PCIe	4-7	Standard
Point-to-point	12-15	ADQ108 Dev Kit
Trigger, Data, Clocks	17-20	ADQ108 Dev Kit
TCLKA	Clk 1	Standard
TCLKB	Clk 2	Standard
FCLKA	Clk 3	Standard

Table 20:

FRONT PANEL ADDITIONAL INTERFACE		
Signal	Connector	Status
1 GbE	SFP	ADQ108 Dev Kit
10 GbE	SFP+	ADQ108 Dev Kit

Figure 11: ADQ108–MTCA card.

Order code: –MTCA

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