ADQ114

ADQ114 is a high speed data acquisition card. The ADQ114 has outstanding dynamic performance from a combination of high bandwidth and high dynamic range, which enables demanding measurements such as RF/IF sampling. Excellent spectral purity in combination with low noise makes ADQ114 ideal for noise measurements.

Introduction

The ADQ114 data acquisition card features single channel, 14 bits resolution, 800 MSPS capture rate with 720 MHz analog input bandwidth, and 128 MSamples memory buffer. The ADQ114 is optimized for spectral purity over a large bandwidth, which makes it ideal for broadband applications such as IF/RF sampling and high-speed data recording. The ADQ114 offers an easy-to-use API that allows easy integration into any application. The card connects to the host via a high-speed USB 2.0 cable or through a Gen1 by 4 lanes cPCIe / PXIe interface, available as an option. The ADQ114 is equipped with two advanced Xilinx V5 series FPGAs that are available for customized real-time applications.

ADQ114 Development Kit

SP Devices' ADQ114 Development Kit is an optional tool for integrating custom real-time signal processing in the FPGA. The custom firmware is easily integrated into the digitizer's standard functions to enhance the capabilities of demanding signal analysis. More details about this product can be found in the datasheet for the ADQ Development Kit.

Ordering information

ORDERING INFORMATION	
ADQ114 USB interface	ADQ114
OPTIONS	
cPCIe / PXIe interface	–PXIE
FPGA upgrade	–SX50T
Positive bias	–PB
Negative bias	–NB
RELATED PRODUCTS	
ADQ114 Development Kit	

Example: ADQ114–PB–PXIE

Features

- 800 MSPS sampling rate
- 720 MHz analog bandwidth
- 14 bits resolution
- Internal and external clock
- External trigger
- Multi record >1 MHz PRF
- Waveform Averaging
- 128 MSamples data memory
- Data interface USB 2.0 / cPCIe / PXIe
- FPGAs open for customized applications

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement

Software support

- C/C++ API
- ADCaptureLab graphical tool
- MATLAB example code
- LabView example code
- Phyton example code
- Windows drivers
- Linux drivers

SWEDEN | Signal Processing Devices Sweden AB | Teknikringen 6, SE-583 30 Linköping | Phone: +46 (0) 13 4650600 | Fax: +46 (0) 13 991 3044
SWITZERLAND | Signal Processing Devices | 275, Route de Saint-Julien, CH-1258 Perly, Geneva | Phone: +41 78 845 5657
US | Signal Processing Devices Inc. | 71 Commercial Street 270; Boston MA 02109 | Phone: +1 415 533 1341

www.spdevices.com

1 Technical data[1]

KEY PARAMETERS	
Number of channels	1
Digitizer Resolution	14 bits
Sampling rate	800 MSPS
Data memory	128 MSamples
Pre-trigger buffer	Up to batch size
Trigger	Software / External / Edge
Number of GPIOs	5 (1 GPIO, 2 In, 2 Out)
Front panel connectors	SMA / Micro-D Plug 9 way
Clock	Internal / External / Ext ref

ANALOG INPUT		
ENOB @ 70 MHz	11.2	bits
SFDR @ 70 MHz	82	dB
SNDR @ 33 MHz	69	dB
Impedance AC	50	Ω
Bandwidth (–3 dB)	10 – 720M	Hz
Input voltage range	2.2	V_{PP}

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range	–2.5 - +3.3	V
Threshold rising edge	0.5	V
Time resolution	625	ps

TRIGGER OUTPUT		
Output impedance	20	Ω
Output high	2	V
Output low	0.1	V

EXTERNAL CLOCK		
Maximum frequency	400	MHz
Minimum frequency	70	MHz
Signal level (min – max)	0.25 – 2	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	

EXTERNAL REFERENCE		
Frequency	10	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω

INTERNAL CLOCK		
Jitter	400	fs RMS
Internal sampling rate	1600/n, n=2..11	MHz
Clock references source	10 MHz external Internal TCXO	

GPIO		
Output impedance GPIO	30	Ω
Out. imp. dedicated output	100	Ω
Output high (all)	3.2	V
Output low (all)	0.1	V
Input impedance (all)	10	kΩ
Input high (all)	2.3	V
Input low (all)	1	V

POWER SUPPLY		
Supply voltage	12	V
Power consumption	20	W

HI-SPEED USB 2.0 INTERFACE		
Sustained data rate	25	MByte/s
Connector	Mini–B	

DIMENSIONS		
Board size	100 x 163	mm^2
Case size	103 x 166 x 31	mm^3

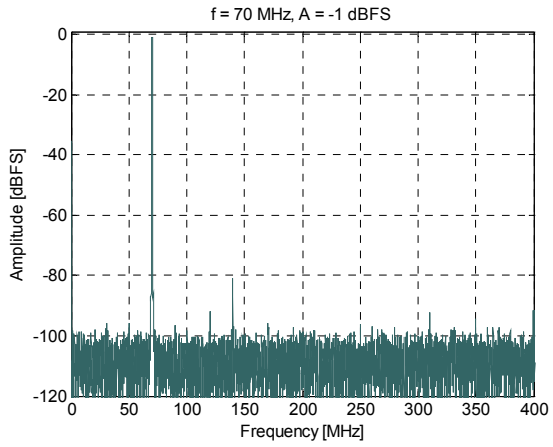
ENVIRONMENTAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	

CERTIFICATION AND COMPLIANCE
CE, FCC 15B

1. All values are typical unless otherwise noted.

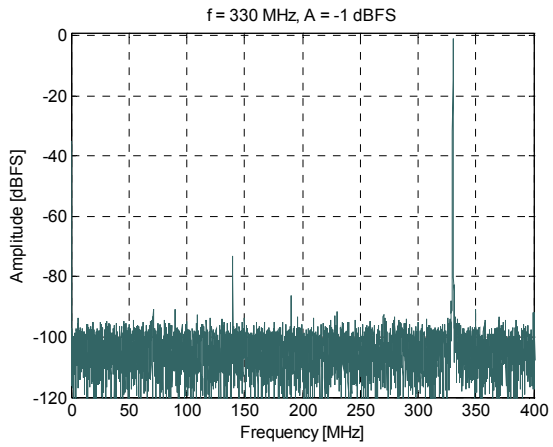
2 Dynamic performance

2.1 Noise and distortion



SFDR	82	dB
SNR	69	dB
ENOB	11.2	bits

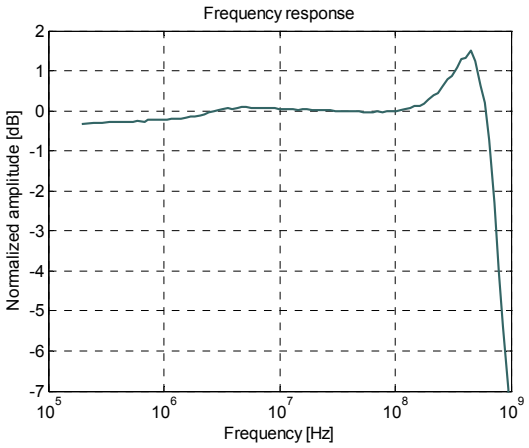
Figure 1: FFT of 70 MHz input signal.



SFDR	73	dB
SNR	65	dB
ENOB	10.5	bits

Figure 2: FFT of 330 MHz input signal.

2.2 Frequency response



Full scale	2.2 V_{PP}
Bandwidth (–3 dB)	720 MHz
1 dB flatness	340 MHz

Figure 3: Frequency response.

3 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (AC)		4.4 V_{PP}
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 °C	45 °C

The ADQ114 has a built-in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ114 from overheating by temporarily shutting down parts of the device.

The SMA connectors has an expected life time of 500 operations. For extensive use, connector savers are recommended.

4 Architecture

4.1 Overview

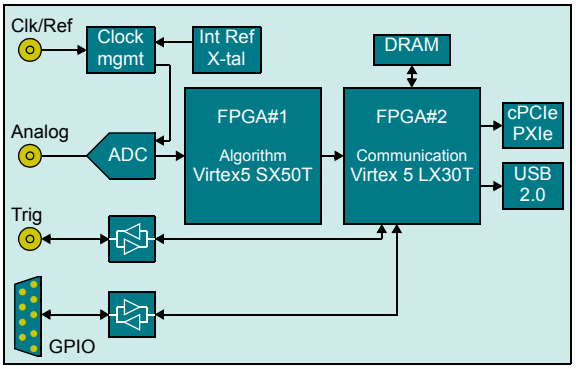


Figure 4: ADQ114 block diagram

4.2 Analog Front End, AFE

The analog input is single-ended AC coupled 50 ohm. The single-ended signal is converted to a differential signal in a balun.

4.3 ADC

The ADC configuration is two 14-bit 400 MSPS ADCs which are time-interleaved to reach 800 MSPS effective sampling rate. The time-interleaving is enabled by SP Devices' time-interleaving algorithm ADX.

4.4 Clock

4.4.1 Clock sources

The clock generator consists of a crystal oscillator as a clock reference and a PLL with built-in VCO. The PLL also has built-in dividers for generating necessary clock frequencies on the board. The sampling frequency is set by configuring these frequency dividers.

There is also an external SMA connector for either an external clock reference or an external clock source.

4.4.2 Setting the sample rate

There are several ways of setting the sample rate.

1. Setting the frequency in the PLL by adjusting the dividers.
2. Applying an external clock.
3. Applying an external reference. This is a fine tuning method, which is specially useful for locking several ADQ114 to the same frequency.
4. Using the sample skip function. The ADCs operate at a sampling rate that is set by any method. The effective sample rate is then reduced by discarding samples in the data stream after the ADC. In this way, very low sampling rates can be achieved and therefore data can be captured during a very long time duration.

4.5 FPGAs

The data outputs of the ADCs are connected to a first Xilinx XC5VSX50T-1 FPGA which runs the time-interleaving algorithm ADX. This FPGA is also open for custom real-time signal processing through the ADQ114 Development Kit. The signal processing in the first FPGA is shown in **Figure 5**.

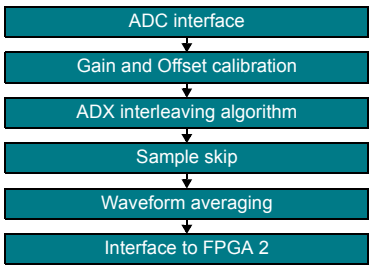


Figure 5: Signal processing

The data is then transferred to a second FPGA, Xilinx XC5VLX30T-1, which handles the communication with the host and the batch data RAM. There is an upgrade option for this second FPGA to an Xilinx XC5VSX50T-1 FPGA which also opens this FPGA for real-time application through the ADQ114 Development Kit, **Section 6.2**.

4.6 Memory

There is 128 MSamples data memory.

4.7 Interface

The communication with the standard ADQ114 take place through USB 2.0 Hi-Speed interface.

See **Section 6.1** for Compact PCI Express (cPCIe) / PXI Express (PXIe) interface.

4.8 Trigger

4.8.1 Overview

The ADQ114 has several trigger options

- Software trigger
- Level trigger
- External trigger

When armed, the system is waiting for the selected trigger event. At the trigger event, a data batch of selected length is recorded in the batch memory. A pre-trigger buffer is available. The length of the pre-trigger buffer is fully controllable. The pre-trigger data is a part of the total batch length.

Example: setting the batch size to 16K samples and pre-trigger to 1K samples gives 1K samples before the trigger event and 15K samples after the trigger event[1].

4.8.2 Software trigger

Data capture is triggered by a software command. This is suitable for measurements on continuous waves.

4.8.3 Level trigger

Data capture is triggered by an event on the input data. This is useful for capturing pulses. The level trigger combined with the pre-trigger buffer setting can capture any pulse shape.

4.8.4 External trigger

Data capture is triggered by positive edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQ114. It is also useful for synchronizing several ADQ114 boards.

The pre-trigger buffer and the trigger hold-off function position the data record in time with respect to the trigger.

1. There is an fixed amount of delay between the trigger and data depending on the length of the wires and the internal signal paths. This delay is fixed for all measurement with the same set-up. The delay might change for a custom application using the ADQ114 Development Kit

The trigger can be configured as a trigger output, **Figure 6**. Use the ADQ114 Development Kit to customize the trigger functions.

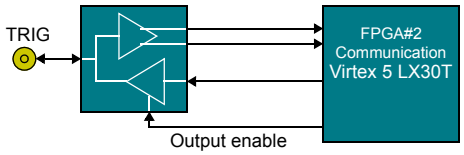


Figure 6: Trig block diagram.

4.9 Multi-record

The ADQ114 can be set up in a multi-record mode. At each trigger, a record of data is recorded in the memory. The length of each record and number of records is user defined.

The pulse repeat frequency (PRF) can be set up to 1.7 MHz depending on the record length. A useful approximation maximum PRF is

$$PRF_{MAX} = \frac{SamplingFrequency}{RecordLength + 512}.$$

PULSE REPEAT FREQUENCY, MULTI RECORD	
Record length	Maximum PRF kHz
16	1700
64	1600
256	1100
1024	550
4096	175
16384	47
65536	12

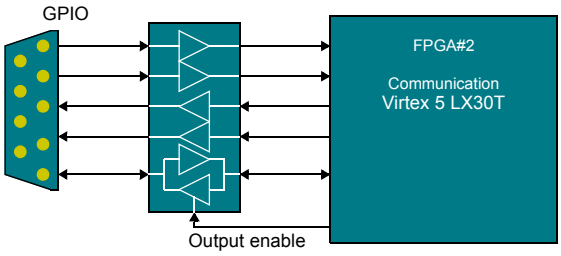
4.10 Waveform averaging

The ADQ114 supports waveform averaging for noise suppression in repeated measurements. Up to 64K records (waveforms) can be averaged in a 32-bit on-board accumulator. The waveform averaging works with external trigger and level trigger.

4.11 GPIO

The ADQ114 is equipped with one bi-directional GPIO, two dedicated inputs and 2 dedicated outputs. The GPIOs are controlled from software, but can also be accessed from the ADQ114 Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.



#	Function
1	In
2	In
3	Out
4	Out
5	GPIO
6	GND
7	GND
8	GND
9	GND

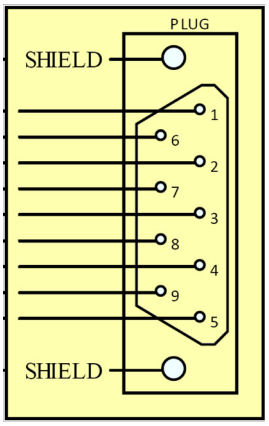


Figure 7: GPIO block diagram.

5 Software tools

5.1 Operating systems

The software package includes drivers for the main operating systems.

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions
Windows 7	32 bit and 64 bit
Windows 8	32 bit and 64 bit
Linux[1]	Kernel 2 and 3, 32 and 64 bits

1. Contact SP Devices sales representative for information about distributions.

5.2 ADCaptureLab

The ADQ114 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time-domain and frequency-domain analysis, see **Figure 8**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ114 operate as a desktop oscilloscope.

Please note that ADCaptureLab is available for Windows only.

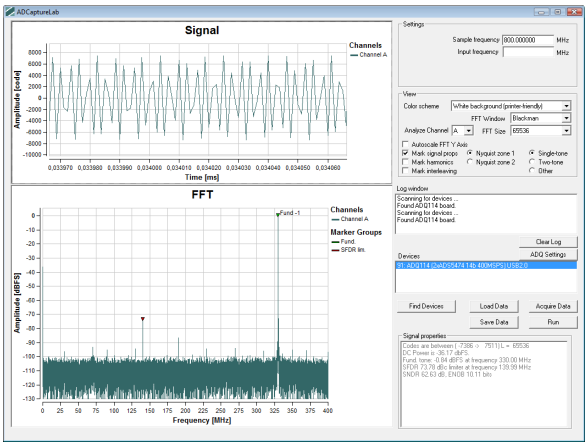


Figure 8: ADCaptureLab (Typical)

5.3 Software development kit (SDK)

The ADQ114 digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ114.

The SDK includes programming examples and reference projects for C/C++ and MATLAB. The ADQAPI users guide in detail describes all functions. Many examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture API, examples
C/C++	Data capture API, examples
Python	Limited example scripts
LabView[1]	Limited support

1. Contact SP Devices sales representative for guidance.

6 Options

6.1 cPCIe / PXIe interface

The ADQ114 is available with cPCIe / PXIe interface supporting Gen1 by 4 lanes.

cPCIe / PXIe INTERFACE		
Bus width	4	lanes
Sustained data rate, 4 lanes	790	MByte/s
PXIe card size	1 slot 3U 4TE	

Figure 9: cPCIe / PXIe interface.

Order code: –PXIE

6.2 FPGA upgrade

The standard configuration for FPGA#2 is a Xilinx Virtex 5 LX30T-1 FPGA.

However, for demanding real-time signal processing applications using the ADQ114 Development Kit[1], an FPGA upgrade to Xilinx Virtex 5 SX50T-1 is available. 90% of the DSP elements and 50% of the logic in this FPGA is then available for the user's custom real-time processing.

Order code: –SX50T

6.3 Biased AC-coupled front end

For unipolar signals, a biased front-end is available. It places the zero level at a pre-biased level and the entire signal range can be used to measure the pulses.

A positive bias (for negative pulses) is available at 90% of the signal range.

Order code: –PB

A negative bias (for positive pulses) is available at 10% of the signal range.

Order code: –NB

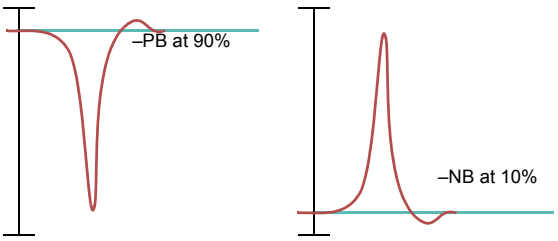


Figure 10: Bias option

1. The ADQ114 Development Kit is a separate tool and not included in the FPGA upgrade option.

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www.spdevices.com

SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com