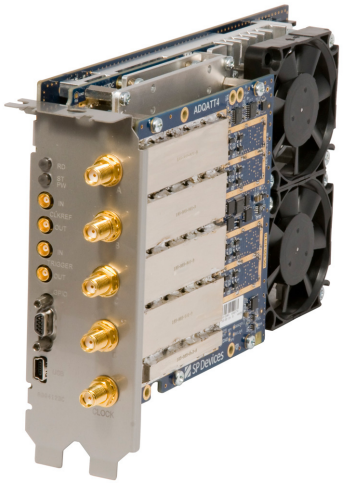
ADQ412DC

The ADQ412DC is the most versatile 12 bits, 4 channels member of the ADQ V6 Digitizer family. Featuring a wide selection of sample rates and form factors in combination with a flexible programmable DC-coupled analog front-end, ADQ412DC meets the requirements of a large variety of detectors in the most advanced measurement situations. The outstanding dynamic performance of ADQ412DC makes it suitable for pulse capture applications as well as RF/IF sampling.



Introduction

The ADQ412DC is designed to meet the demands from a large variety of advanced systems. The flexibility is represented in three ways; front-end flexibility for adaptation to sensors, sample rate options for acquisition requirements, and host interface options for optimal systems design.

The flexible DC-coupled analog front end contains a variable gain, variable bias control, over voltage protection and anti-aliasing noise suppression filter.

The ADQ412DC is available in several sample rates from 1 GSPS up to 4 GSPS per channel and can be configured either as 2 or 4 analog input channels through a software control.

The ADQ412DC is available in cPCIe / PXIe form factor for modular instrumentation and in PCIe form factor for compact integration in a PC.

The ADQ412DC offers an easy-to-use API that allows easy integration into any application. A firmware development kit, ADQ412DC Development Kit enables real time signal processing in the FPGA.

ADQ412DC Development Kit

The ADQ412DC is equipped with an powerful Xilinx V6 LX240T FPGA which is partly available for customized real time applications.

SP Devices' ADQ412DC Development Kit is an optional tool for integrating custom real-time signal processing in the FPGA. The custom firmware is easily integrated into the digitizer's standard functions to enhance the capabilities of demanding signal analysis. More details about this product can be found in the datasheet for the ADQ Development Kit.

Features

- Up to 4 analog channels
- Up to 4 GSPS sample rate per channel
- 12 bits vertical resolution
- DC to 925 MHz analog BW
- Internal and external clock reference
- Internal and external clock source
- Clock reference output
- Internal and external trigger
- Trigger output
- Multi record >1 MHz PRF
- Time stamp
- 700 Msamples data memory
- Data interface cPCIe / PXIe / PCIe
- FPGA open for custom applications

Applications

- RADAR
- LIDAR
- Wireless communication
- High-speed data recording
- Test and measurement
- Fast pulse capture

Ordering information

ORDERING INFORMATION	
Order code	ADQ412DC
AVAILABLE OPTIONS	
cPCIe / PXIe interface	–PXIE
PCIe interface	–PCIE
Sampling rate 1/2 GSPS	–1G
Sampling rate 1.8/3.6 GSPS	–3G
Sampling rate 2/4 GSPS	–4G
RELATED PRODUCTS	
ADQ412DC Development Kit	

1 Technical data[1]

Table 1:

KEY PARAMETERS OVERVIEW	
Vertical resolution	12
Analog channels	2 / 4
Signal range settings	100 mV_{pp} to 5 V_{pp}
Range setting step size	0.25 dB
Bias settings	Full signal range
Bias setting steps	3000 levels
Sample rate per channel	Up to 4 GSPS, see below
Impedance DC	50 Ω
Over voltage protection[1]	10 V_{pp}
Analog bandwidth	DC–1700 MHz

1. See Absolute maximum rating, **Section 6**.

Table 2:

SAMPLE RATE OPTIONS (PER CHANNEL)	–1G	–3G	–4G	
4 CHANNELS MODE				
Number of channels	4	4	4	
Sampling rate	1	1.8	2	GSPS
Analog BW	850	850	850	MHz
2 CHANNELS MODE				
Number of channels	2	2	2	
Sampling rate	2	3.6	4	GSPS
Analog BW	775	775	775	MHz

Table 3:

AC DATA 32 MHZ 4 CH 1.8 GSPS					
RANGE	SNR	SINAD	THD	SFDR	ENOB
100 mV_{pp}	49	49	–61	64	7.9
200 mV_{pp}	54	53	–63	65	8.5
1 V_{pp}	54	54	–64	65	8.6
5 V_{pp}	54	54	–64	65	8.6

Table 4:

AC DATA 32 MHZ 2 CH 3.6 GSPS					
RANGE	SNR	SINAD	THD	SFDR	ENOB
100 mV_{pp}	48	47	–60	52	7.6
200 mV_{pp}	53	53	–64	60	8.5
1 V_{pp}	54	53	–63	60	8.5
5 V_{pp}	53	53	–63	59	8.5

Table 5:

BIAS SETTINGS (EXAMPLES)		
RANGE	MIN	MAX
100 mV_{pp}	–50 mV	50 mV
200 mV_{pp}	–100 mV	100 mV
1 V_{pp}	–0.5 V	0.5 V
5 V_{pp}	–2.5V	2.5V

Table 6:

GPIO		
Number of GPIO	5	
Output impedance pin #5	33	Ω
Output impedance Pin #1–4	100	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	Micro DSUB 9 way	

Table 7:

EXTERNAL CLOCK SOURCE		
Frequency 4 channels mode	FS	MHz
Frequency 2 channels mode	FS/2	MHz
Signal level (min – max)	0 – 10	dBm
	0.64 – 2	Vpp
Impedance AC	50	Ω
Duty cycle	50%	
Connector	SMA	

Table 8:

CLOCK REFERENCE INPUT		
Internal clock reference		
Frequency	10	MHz
Accuracy	± 5 ± 0.5/y	ppm
External clock reference		
Frequency (min – max)	1 – 250	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector	MCX	
PXIe clock reference[1]		
PXIe clock	100	MHz
PXIe sync[2]	10	MHz

1. Available on PXIe form factor only
2. Jitter reduced by PXIe clock in digitizer

1. All values are typical unless otherwise noted.

Table 9:

CLOCK REFERENCE OUTPUT		
Frequency	Set by clock reference	
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector	MCX	

Table 10:

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–0.4 to 2.4	V
Threshold rising/falling edge	500	mV
Sensitivity	200	mV
Jitter	25	ps
Resolution	1/FS	s
Connector	MCX	

Table 11:

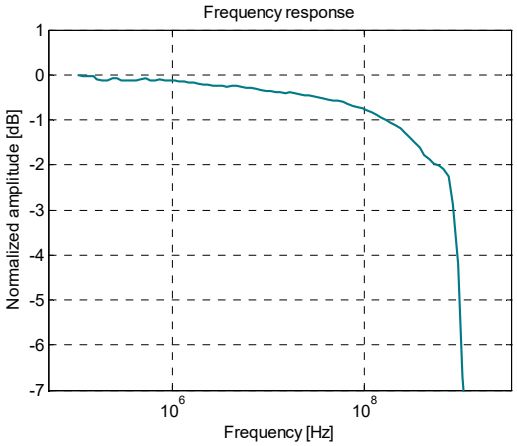
TRIGGER OUTPUT		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Connector	MCX	

Table 12:

POWER SUPPLY		
Supply Voltage	12	V
Power	43	W
Connector PCIe	6-pin ATX power	
Connector cPCIe/PXIe	from slot	

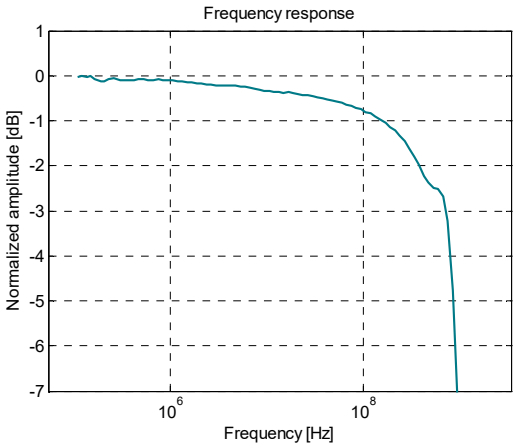
2 Dynamic performance

2.1 Frequency response



Bandwidth (–3 dB)	850 MHz
1 dB flatness	160 MHz

Figure 1: Frequency response in 4 channels mode.



Bandwidth (–3 dB)	720 MHz
1 dB flatness	150 MHz

Figure 2: Frequency response in 2 channels mode.

2.2 Dynamic performance

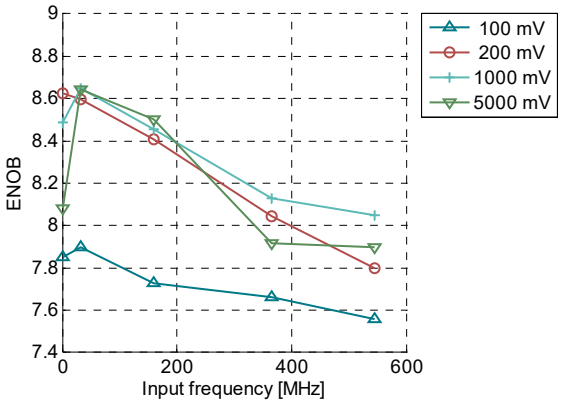


Figure 3: ENOB, 1.8 GSPS in 4 channels mode.

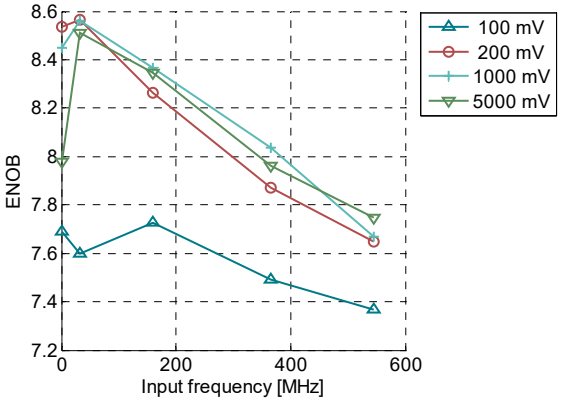


Figure 6: ENOB, 3.6 GSPS in 2 channels mode.

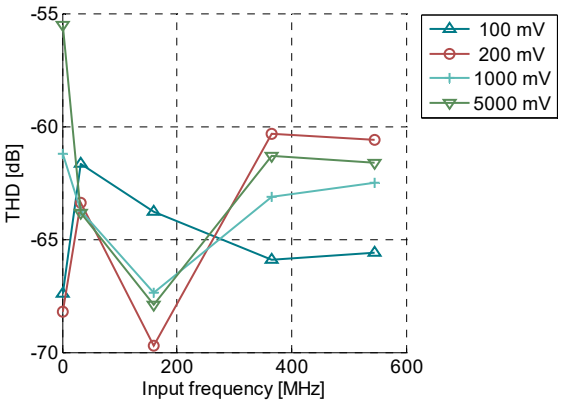


Figure 4: THD, 1.8 GSPS in 4 channels mode.

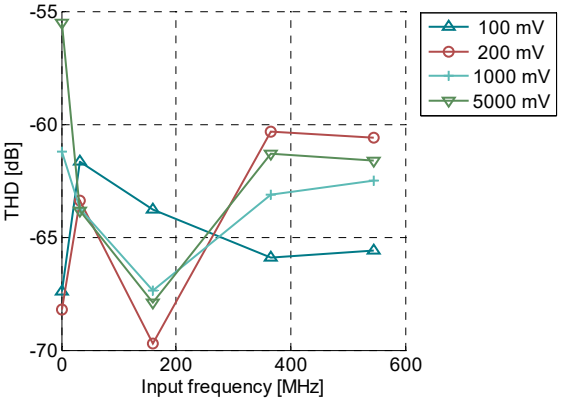


Figure 7: THD, 3.6 GSPS in 2 channels mode.

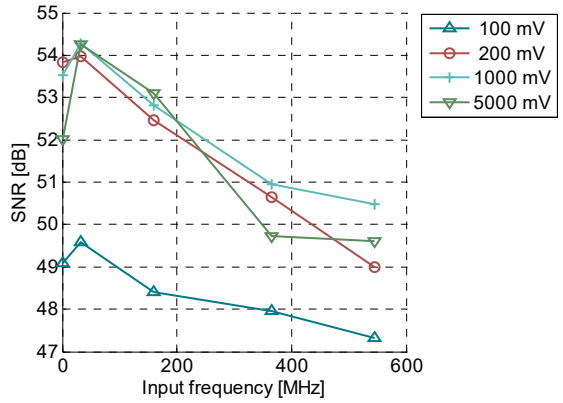


Figure 5: SNR, 1.8 GSPS in 4 channels mode.

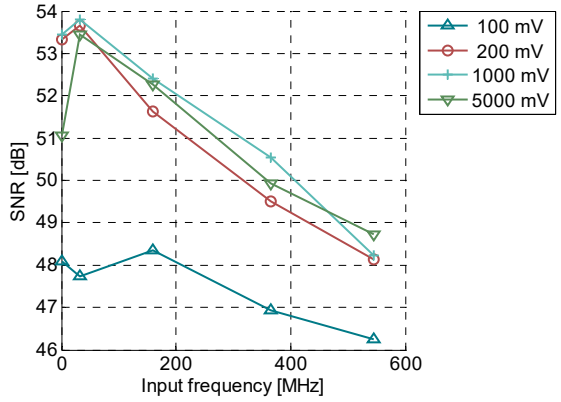
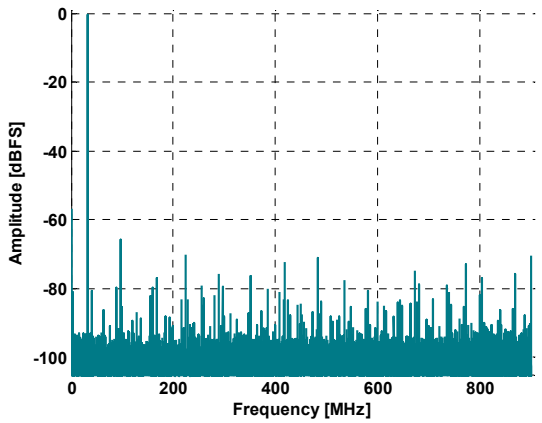


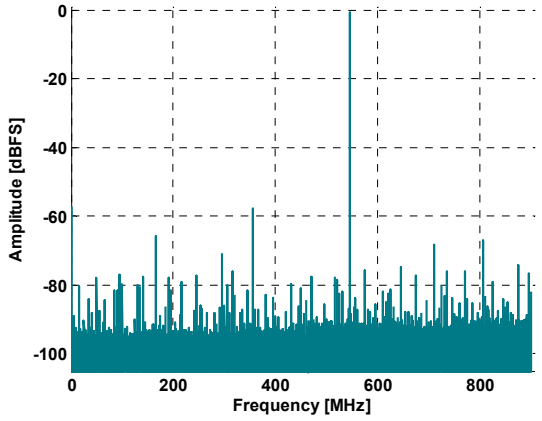
Figure 8: SNR, 3.6 GSPS in 2 channels mode.

2.3 Frequency domain



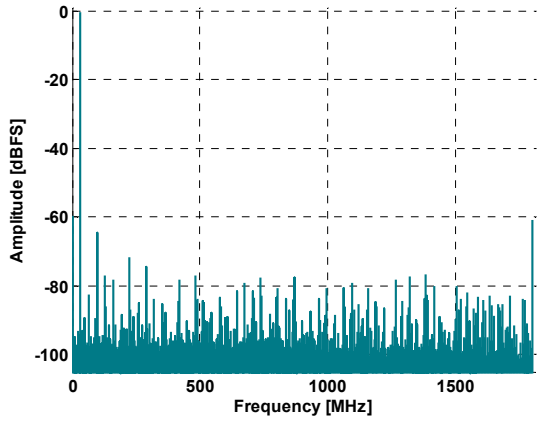
Sampling frequency	1.8 GSPS
Mode	4 channels
Input signal frequency	32 MHz
Input signal range	1 V_{pp}

Figure 9: Frequency domain.



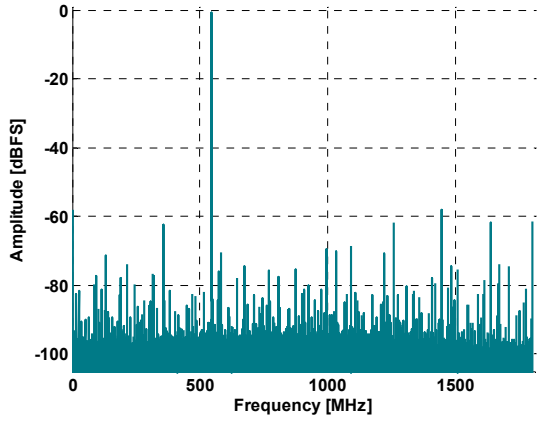
Sampling frequency	1.8 GSPS
Mode	4 channels
Input signal frequency	545 MHz
Input signal range	1 V_{pp}

Figure 10: Frequency domain.



Sampling frequency	3.6 GSPS
Mode	2 channels
Input signal frequency	32 MHz
Input signal range	1 V_{pp}

Figure 11: Frequency domain.



Sampling frequency	3.6 GSPS
Mode	2 channels
Input signal frequency	545 MHz
Input signal range	1 V_{pp}

Figure 12: Frequency domain.

3 Functional overview

3.1 Block diagram

The digitizer includes an analog front-end with signal conditioning and A/D conversions and a digital back-end for data flow control, triggering and host communication, see **Figure 13** and **Figure 14**.

3.2 Analog front-end

The ADQ412DC can operate in a 4 channels mode where each ADC is connected to one analog input channel, **Figure 13**. In the 2 channels mode, two ADCs operate on the same analog input in an interleaved mode, **Figure 14**. This doubles the sampling rate. The interleaving is enabled by ADX, see **Section 3.3**. Switching between 2 and 4 channels mode is software controlled.

The analog front end contains over-voltage protection, variable gain setting and variable DC bias, and noise suppression filter, **Figure 15**. The gain is set in steps of 0.25 dB to get any full scale signal range from 100mV$_{pp}$ to 5V$_{pp}$. The bias is set in 3000 steps and the range is covering the selected gain setting. The settings are user controlled via software.

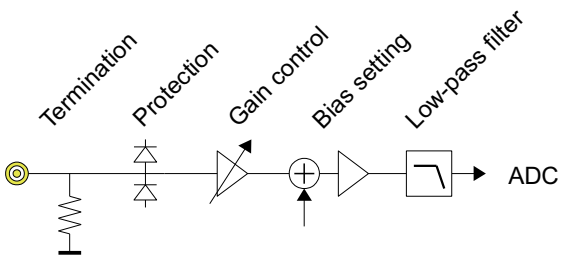


Figure 15: Flexible analog front-end

3.3 Interleaving ADX

The high data rate in 2-channel mode is enabled by SP Devices' proprietary technology for interleaving of ADCs: ADX.

3.4 Data recording

There are several methods for data recording to serve different use cases;

- Multi-record recording in on-board DRAM for very long records.
- Triggered streaming for fast data transfer and long measurement time.
- Individual level trigger for multi-channel pulse capture

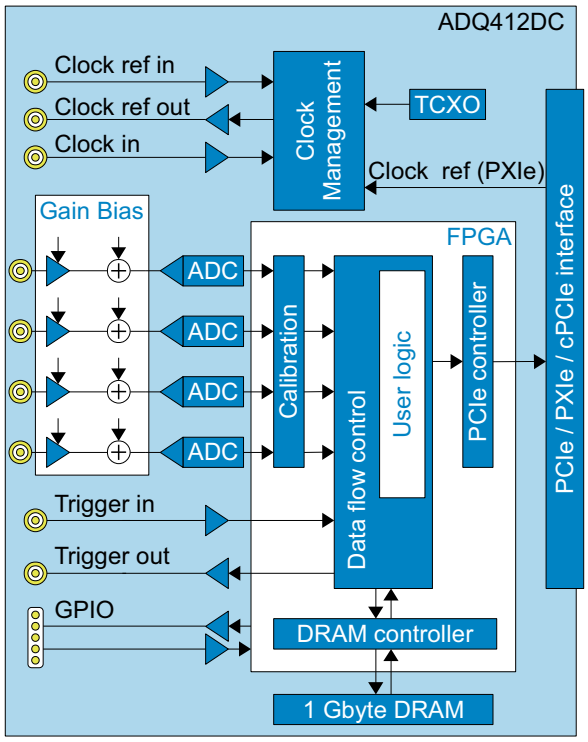


Figure 13: Block diagram 4 channels mode.

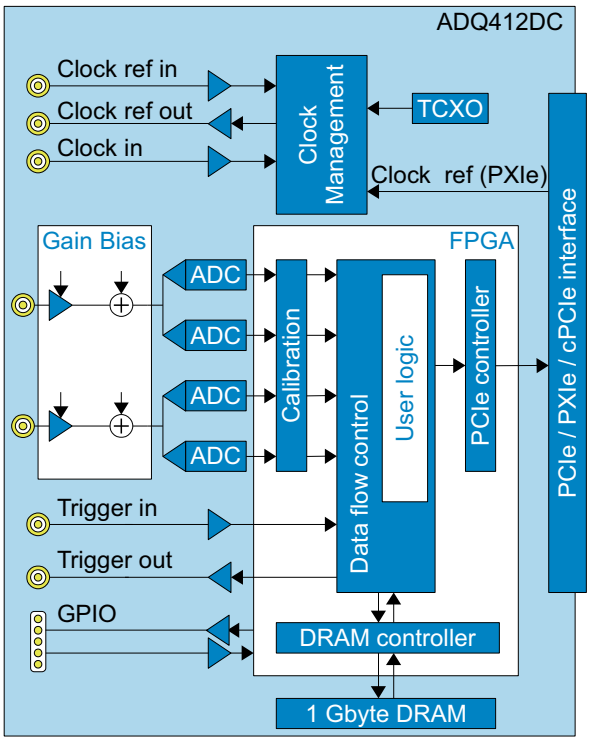


Figure 14: Block diagram 2 channels mode.

- Continuous multi-record via on-board DRAM for acquisition of long records during long measurement time.[1]
- Continuous streaming of data to the host PC for real time analysis of data[2]

To support data recording, there is on board DRAM of 1 GBytes. The interface to the host PC enables up to 3.2 GBytes/s over a Gen2 x8 PCIe interface.

3.5 Signal processing

There is support for real time signal processing on the digitizer;

- Real time waveform averaging.
- Level trigger for event detection.
- Gain and offset calibration.
- Custom real time signal processing can be implemented using the ADQ412DC Development Kit.

3.6 Trigger

There are several trigger modes;

- External for synchronization
- Level trigger for data driven acquisition
- Software for user's control
- Internal for automatic sequencing

There is also a trigger output for triggering external equipment. The trigger timing is controlled by pre-trigger buffer and trigger delay parameter settings.

3.7 Clock

There are several modes for clocking the digitizer

- Internal clock for stand alone operation
- External clock for synchronization
- External clock reference for synchronization

There is also a clock reference output for clocking external equipment.

3.8 GPIO

There are 5 GPIO for real time communication with external equipment. The GPIOs are controlled from software, but can also be accessed from the ADQ412 Development Kit for integration in a real time control system.

1. Option. Contact an SP Devices' sales representative for more details.
2. This mode required ADQ412DC Development Kit for data rate reduction.

GPIO pin #2 may also be used for time stamp synchronization signal. See **Section 7.5**.

The connector is Micro DSUB plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.

#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

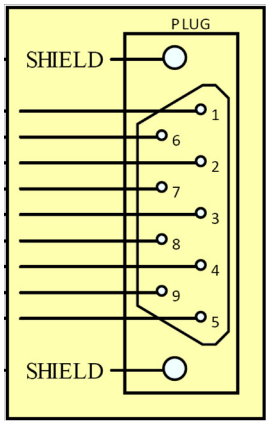


Figure 16: GPIO connector.

4 Calibration

The ADQ412DC is calibrated in factory.

5 Front panel

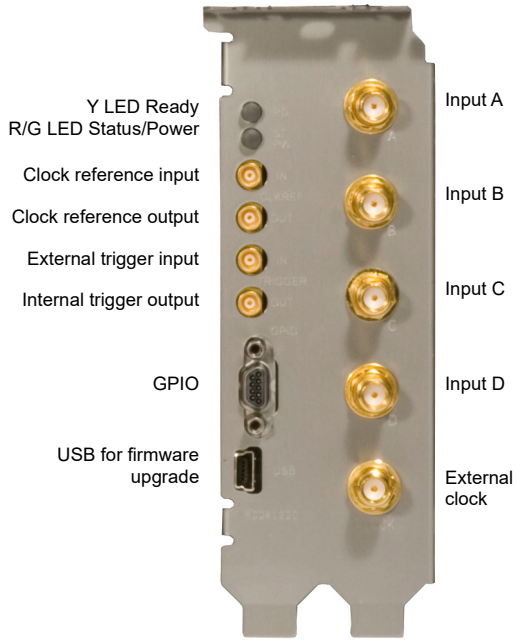


Figure 17: ADQ412DC–PCIE front panel.

6 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device.

The ADQ412DC has a built-in fan to cool the device. The built in temperature surveillance unit will protect the ADQ412DC from overheating by shutting down parts of the device in such a situation.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

Table 13:

ABSOLUTE MAXIMUM RATINGS	MIN	MAX
Supply voltage (to GND)	–0.4 V	14 V
Trigger input (to GND)	–3 V	3.7 V
Clock ref (AC)		3.3 V_{PP}
GPIO input (to GND)[1]	–1 V	4.6 V
Ambient temperature (operation)	0 °C	45 °C
Analog inputs		
DC, see **Figure 18**.	–5 V	5 V
	–160 mA	160 mA
AC, see **Figure 18**.		10 V_{pp}
	–160 mA	160 mA

1. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

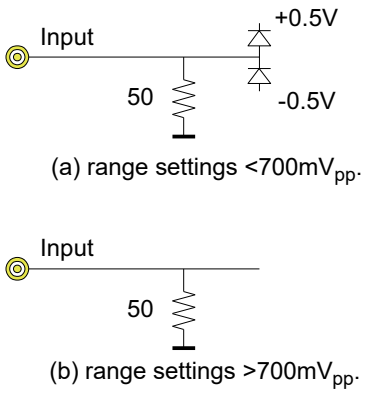


Figure 18: Equivalent circuit for the analog input

7 Software tools

7.1 Operating systems

The software package includes drivers for the main operating systems.

Table 14:

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions
Windows 7	32 bit and 64 bit
Windows 8	32 bit and 64 bit
Linux[1]	Kernel 2 and 3, 32 and 64 bits

1. Contact SP Devices sales representative for information about distributions.

7.2 ADCaptureLab

The ADQ412DC is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 19**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ412DC operate as a desktop oscilloscope.

Please note that ADCaptureLab is available for Windows only.

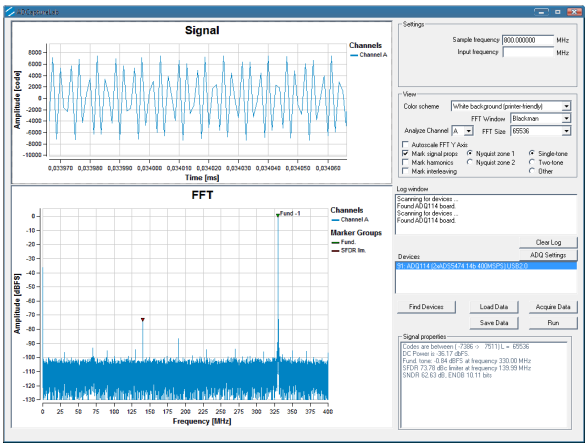


Figure 19: ADCaptureLab (Typical)

7.3 Software development kit (SDK)

The ADQ412DC digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ412DC.

The SDK includes programming examples and reference projects for C/C++ and MATLAB. The ADQAPI users guide in detail describes all func-

tions. Many examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

Table 15:

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture API, examples
C/C++	Data capture API, examples
Python	Limited example scripts
LabView[1]	Limited support

1. Contact SP Devices sales representative for guidance.

8 Sample rate options

The ADQ412DC is available with several sample rates options. See **Section 1** for technical data on the different options.

The order code for option 1/2 GSPS[1] per channel is

Order code: –1G

The order code for option 1.8/3.6 GSPS per channel is

Order code: –3G

The order code for option 2/4 GSPS per channel is

Order code: –4G

1. The notation denotes sample rate for different modes of operation. For example, 1/2 GSPS means 1 GSPS per channel in 4 channels mode and 2 GSPS per channel in 2 channels mode.

9 Data interface options

9.1 CompactPCI Express / PXI Express

The ADQ412DC is available in a form factor for modular instrumentation in a Compact PCI Express or PXI Express chassis.

Table 16:

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Sustained data rate	3.2	GByte/s
PXIe card size	3U 2 slot 8TE	

Figure 20: ADQ412DC–PXIE.

Order code: –PXIE

9.2 PCI Express interface

The PCI Express interface is intended for integration in a PC.

Table 17:

PCIe INTERFACE		
Data rate	Gen2	
Bus width electrical	8	lanes
Sustained data rate, 8 lanes	3.2	GByte/s
Bus width mechanical[1]	16	lanes
Board height	2	slots
Board length (Short)	167	mm

1. The wide contact is required to support the weight of the board.

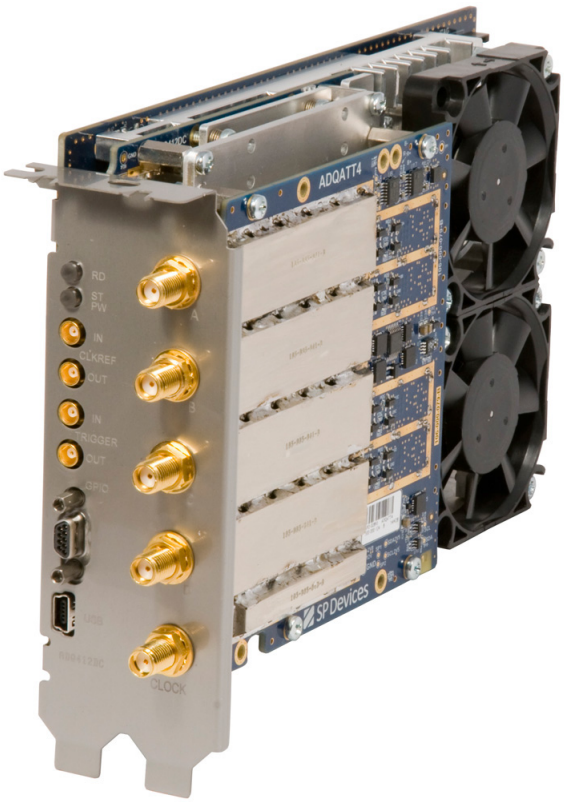


Figure 21: ADQ412DC–PCIE.

Order code: –PCIE

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