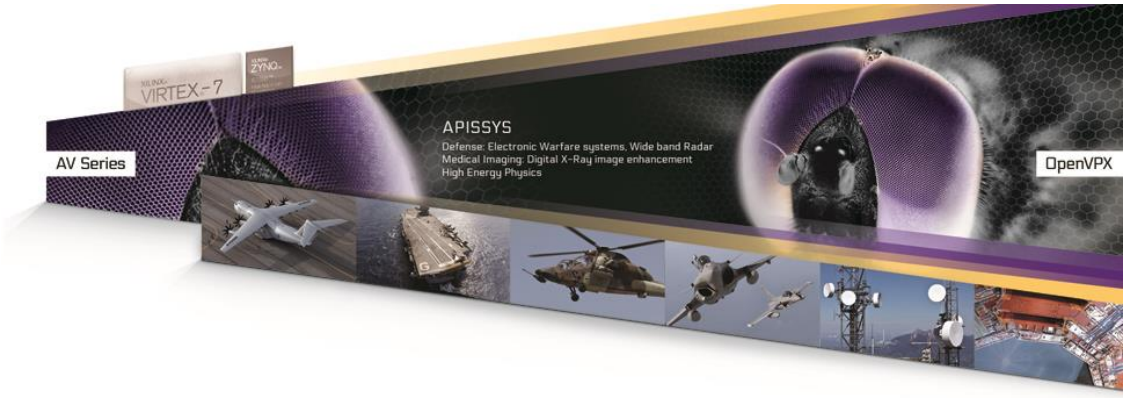
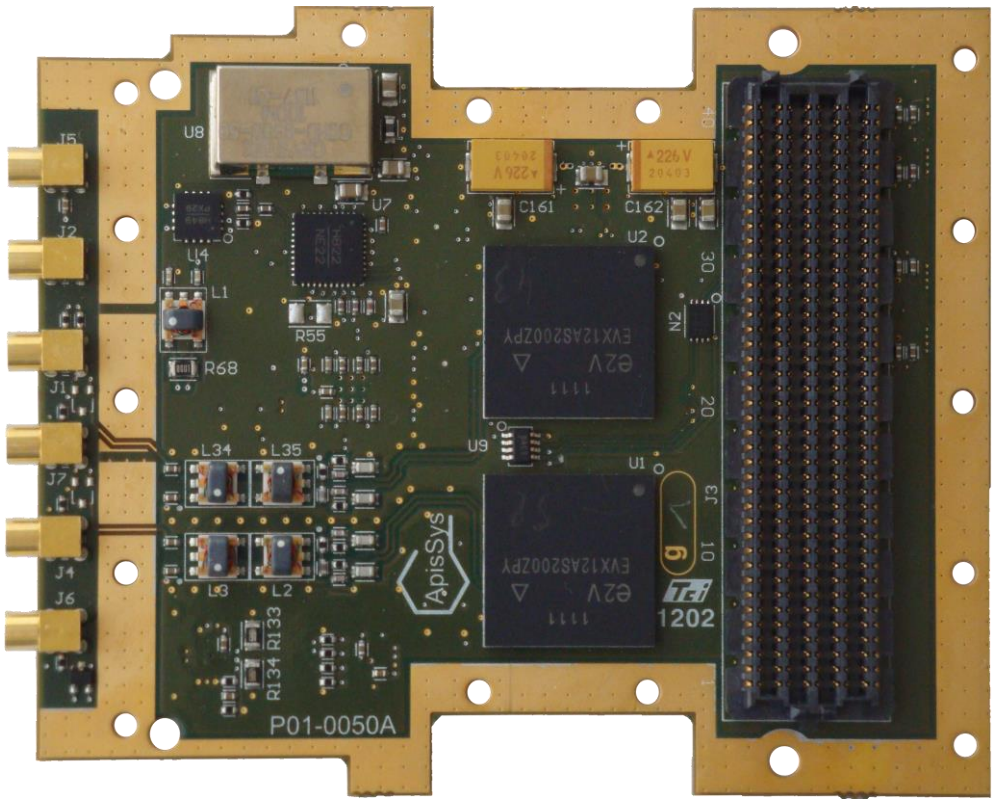


AF202

Dual Channel 12-bit 1.5 GSPS ADC FMC



Applications

- Test & Measurement
- Electronic Warfare
- Radar Receiver
- Software Defined Radio

Features

- 2 channels 12-bit, 1.5 Gsps ADC
- External clock and reference input
- Internal low jitter clock generation
- External trigger input
- VITA 57 FMC form factor
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

Overview

The AF202 is part of ApisSys' range of modular IOs solutions based on the VITA 57, FPGA Mezzanine Card standard.

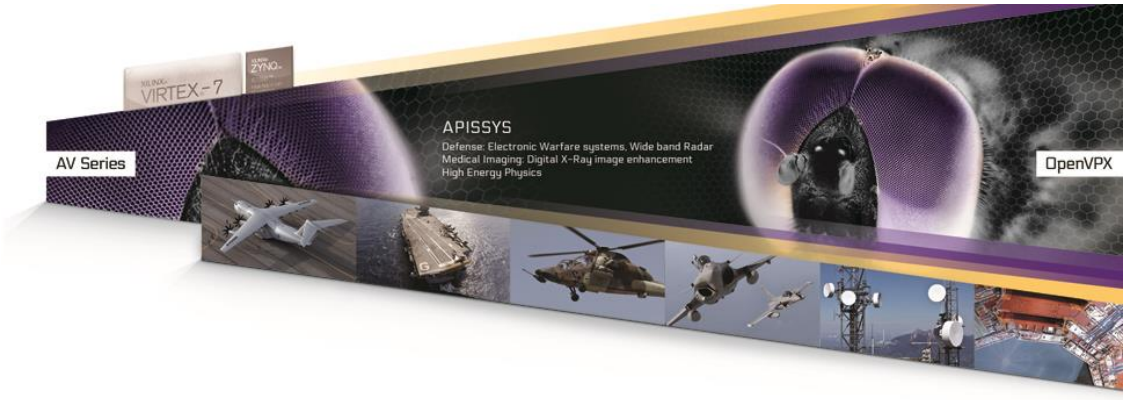
The AF202 provides customers with a dual channel 12-bit up to 1.5 Gsps ADC capability, ideally suited for test and measurement, Software Defined Radio or Radar Receivers applications.

The AF202 ADC channels are AC coupled with an input bandwidth wider than 2.3 GHz for a full scale signal of 2 dBm (800 mVpp).

The AF202 provides an internal ultra low jitter clock generation and can be used with either an external clock or an external reference for higher flexibility.

The AF202 features an external trigger input used to synchronize processing with external events.

The AF202 is fully supported on ApisSys 3U VPX FPGA processing engines, making it ideally suited for test and measurement, Electronic Warfare, Ultra Wideband Radar Receivers or LIDAR applications.



12-bit 1.5 GSPS ADCs

The AF202 Analog to Digital conversion is performed by two e2v EV12AS200 12-bit 1.5 Gsps ADCs.

The AF202 provides one front panel MMCX connector for each analog input.

Input signals are single ended AC coupled with an input bandwidth from 5 MHz to more than 2.3 GHz with 2 dBm input level.

Clock

The AF202 provides an internal ultra low jitter clock generator locked on a 100 MHz internal reference.

The AF202 provides a front panel MMCX connector for an external reference from 10 to 100 MHz, a front panel MMCX connector for an external clock input from 500 MHz to 1.5 GHz and a front panel MMCX connector for an external clock output.

Estimated jitter from the internal clock generation (including 100 MHz reference and clock distribution) is below 200 fs for a 1.5 GHz clock. Added jitter on external clock is lower than 100 fs.

Trigger and Synchronization

The AF202 provides a front panel MMCX connector for external trigger input.

The trigger mechanism provides the customer with a one sample event resolution, allowing for multiple channel fine synchronization using an external clock and trigger distribution board.

FMC interface

The AF202 features a VITA 57 – FMC (FPGA Mezzanine Card) compliant slot.

The FMC uses High Pin Count (HPC) interface with 2.5V Vadj.

The FMC MGT interfaces are unused.

Firmware

The AF202 comes with a firmware package which includes VHDL cores allowing control and communication with all AF202 hardware resources.

A base design is provided which demonstrates the use of the AF202 and gives users a starting point for firmware development.

The AF202 firmware package is supported on the Xilinx ISE® 13 design suite and later versions.

The AF202 firmware package has been fully validated on AV103 and other ApisSys FMC carrier products.

Software

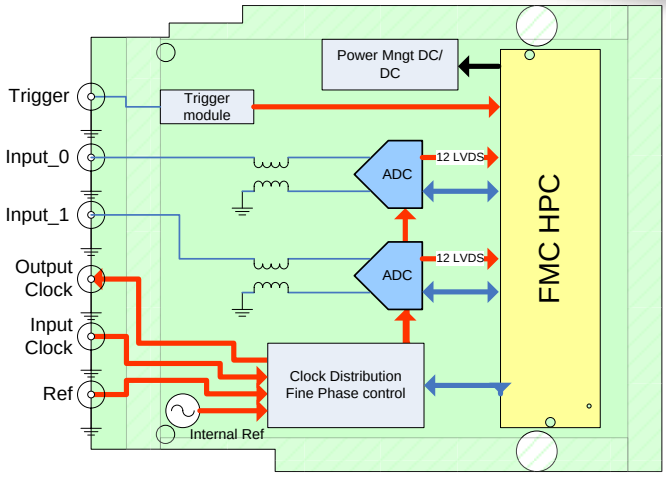
The AF202 is delivered with control software for Windows XP and 7, and Linux, compatible with AV103 and other ApisSys FMC carrier products.

An application example is provided as source code.

Ruggedization

The AF202 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC3.



Specifications

Analog Inputs

- Input coupling: AC
  - Full power bandwidth > 2.3 GHz
  - Full scale : 2 dBm
- Impedance: 50 Ohm
- Connector: MMCX

Analog to Digital Conversion

- Dual channel
- Resolution: 12 bit
- Sampling Frequency (assembly option):
  - 1.33 to 1.5 GHz
  - 1.285 to 1.415 GHz

Sampling Performances

- 1.5 Gsps, Fin = 500 MHz, -1dBFS:
  - SNR: 55 dBFS
  - SFDR: 63 dBc
  - ENOB: 8.7 bits
- 1.5 Gsps, Fin = 1 GHz, -1dBFS:
  - SNR: 57 dBFS
  - SFDR: 60 dBc
  - ENOB: 8.9 bits
- 1.5 Gsps, Fin = 1.5 GHz, -1dBFS:
  - SNR: 55 dBFS
  - SFDR: 67 dBc
  - ENOB: 8.7 bits

Clock

- Internal low jitter clock (assembly option):
  - 1.33 to 1.5 GHz GHz
  - 1.285 to 1.415 GHz
  - Internal jitter: < 200 fs
- External Input Clock:
  - frequency: 500 MHz to 1.5 GHz
  - Level: 10 dBm to 15 dBm
  - Added jitter (Ext clock) < 100 fs
  - Connector: MMCX, 50 Ohm
- External Output Clock:
  - frequency: sampling clock
  - Level: 0 dBm
  - Connector: MMCX, 50 Ohm
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Level: 10 dBm to 15 dBm
  - Connector: MMCX, 50 Ohm

Trigger

- External: 0 to 2Vp
  - Connector: MMCX

FMC interface

- HPC:
  - LA(0:33): LVDS 2.5V
  - HA(0:23): LVDS 2.5V
  - HB(0:21): LVCMOS 2.5V

Software support

- Software Drivers:
  - Windows XP and 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx ISE 14 and later

Ruggedization

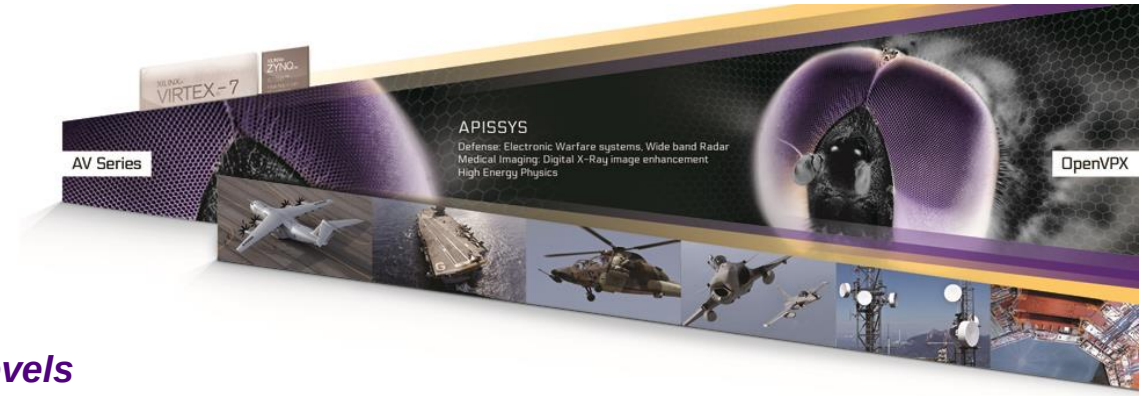
- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3

Power dissipation

- +12V: 1.0 A max (12W)
- +3.3V: < 0.1 A
- VADJ (2.5V): 0.6 A max (1.5W)
- +3.3VAUX: < 0.1 A

Weight

- Air cooled : 50g
- Conduction cooled : 55g



Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (1) (8 CFM airflow at sea level)	-40 to +70ºC (1) (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.04 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz - 1kHz = 0.1 g2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic 1B31)	Yes (default acrylic 1B31)	Yes (default acrylic 1B31)

Ordering information

Part Number		A F 202 -	rr	-	a
Ruggedization level	Air Standard		AS		
	Air Rugged		AR		
	Conduction Standard		CS		
	Conduction Rugged		CR		
Options 1	1.33 to 1.5 GHz internal clock				1
	1.285 to 1.415 GHz internal clock				2

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