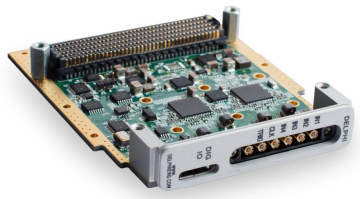

ADF-D3030

Dual 3.0 Gsps, 14-bit ADC and Dual 3.0 Gsps 16-bit DAC FMC Module. VITA 57.1

The ADF-D3030 FMC module from DEG is a highly integrated, dual channel ADC and dual channel DAC FMC module. The AD9208 from Analog Devices delivers 14 Bit resolution at sample rates of up to 3.0 Gsps. The DAC is an Analog Devices AD9172. This 16 Bit DAC device operates at 3.0 Gsps natively and up to 12.0 Gsps in interpolation mode. A VITA 57-compliant FPGA Mezzanine Card (FMC) interface, the ADF-D3030 offers industry-wide platform compatibility with the PCIe/VME/VXS/VPX carrier board of your choice. The ADF-D3030 and associated HDL firmware are compatible with Xilinx® FPGA processors.

BENEFITS

- Dual ADC/DAC on a Single FMC Module
- Wide Dynamic Range for both ADC and DAC
- Convection and Conduction-Cooled Versions
- Enables SWaP-C Sensitive Systems: High Density, Small Footprint, Low Power

FEATURES

- Dual Channel 3.0 Gsps 14-bit ADC
- Dual Channel 3.0 Gsps 16-bit DAC : 12 GHz in Interpolation Mode
- JESD204B SERDES Interface: x 8 Lanes DAC and x8 Lanes ADC @ 15.0 Gbs per Lane
- Built-in Clock Jitter Cleaner
- Four Internal Digital Down-Converters per ADC Channel

ADC PERFORMANCE

- Up to 5 GHz of usable analog input full power bandwidth – AC Coupled.
- ENOB = 9.5 effective bits, F_{in} = 765 MHz
- SNR = 58.8 db @ F_{in} = 765 MHz
- SFDR = 71 dB @ F_{in} = 765 MHz

Flexible, cost-effective solution

By coupling this core architecture with the compact and flexible FMC form factor, DEG has enabled customers to rapidly and cost-effectively build compact systems with significant SWaP-C benefits. By incorporating two channels of both high speed ADC and DAC on a single FMC module, high-channel density, wideband digital receivers can be incorporated into the latest generation of high-performance sensor and EW systems. This flexible approach reduces the overall power consumption and cost while increasing ruggedness and reliability.

The ADF-D3030 is ideally suited for low latency EW applications and signal intelligence systems that require wide dynamic range and high sensitivity.

Performance

The ADF-D3030 incorporates the JESD204B SERDES Interface standard. The ADC and DAC each utilizes 8 lanes to and from a carrier board FPGA. Sustained data transfer rates of 15.0 Gbytes/sec. are supported.

Clocks

The ADF-D3030 provides an onboard synthesizer which covers the entire ADC and DAC sampling range. Delphi incorporates a clock jitter cleaner on the ADF-D3030, which improves ADC and DAC performance.

The following sources can be selected for the synthesizer:

- External reference signal
- Low noise onboard reference – 50 ppm accuracy over the entire temperature range of the product

External Clock via front-panel clock input

Trigger

A trigger event is initiated by a positive transition. The trigger threshold is software-controllable in a wide range. An auto-trigger feature enables signal capture or synthesis without a trigger.

ADCLink

Delphi's ADCLink VHDL source code provides the specific ADC/ DAC interface and control logic necessary to integrate with your carrier board FPGA.

ADCLink capabilities include: onboard/external reference clock control, trigger threshold control, and full control over ADC and DAC devices.

ADF-D3030 Performance Specification

ADC Specifications	
Number of ADC channels	2
Sampling Rate Options	2500 to 3100 Msps, 1900 to 2600 Msps 1300 to 2100 Msps
Input Bandwidth	3.0 GHz
Input Impedance	50 Ω, AC-coupled
SNR (typical)	58.8 dB @ F_{in} = 765 MHz
SFDR (typical)	71.0 dB @ F_{in} = 765 MHz
ENOB (typical)	9.5 Bits @ F_{in} = 765 MHz
DAC Specifications	
Number of DAC channels	2
Sampling rate	3.0 Gsps
Sampling rate	12.0 Gsps (w/Interpolation)
Output bandwidth	6.0 GHz
Output impedance	50 Ω, AC-coupled
Clock and Trigger Specifications	
External Clock Input Freq.	3.0 - 12.0 GHz
Ext. Reference Clock Input	10 MHz to 750 MHz
Trigger input	Single-ended 50 Ω