Virtex™-5 Product Overview

Xilinx Virtex™-5 Platform FPGA Boards

Xilinx Virtex-5 FPGA
A new generation of reconfigurable computing performance

Analog I/O, Camera Link, LVDS, FPDP-II & RS422/485
Fast, integrated I/O without bottlenecks

Multiple banks of fast memory
DSP and I/O optimized memory architecture

PCI-X interface with multiple DMA controllers
More than 1 GByte/s host bandwidth

Rich set of development tools and utilities
For rapid application development

Applications
- Electronic Warfare
- Electro-Optics
- Radar/Sonar
- Signal Intelligence
- Software Defined Radio
- Imaging
Introduction

VMETRO New Generation FPGA Products

VMETRO has nearly a decade of experience creating leading edge commercial off-the-shelf (COTS) FPGA products for embedded processing applications. The expertise garnered from supporting each previous FPGA generation is brought to a new family of products based on the flagship field programmable gate array (FPGA) from Xilinx: the Virtex™-5 platform.

The VMETRO product range provides developers with analog input and output, high speed digital data transport and high performance processing solutions.

Virtex-5 FPGAs offer higher density, lower cost per gate and better performance, in more capable devices, than previous generations of FPGA. The enhancements over previous generations give developers the ability to create more effective algorithms, to solve the most demanding real-world problems.

The Virtex-5 family of devices offers four new platforms, each with a different balance of high-performance logic, serial connectivity, signal processing and embedded processing suitable for different application areas:

- Virtex-5 LX: High performance general logic applications
- Virtex-5 LXT: High performance logic with advanced serial connectivity
- Virtex-5 SXT: Signal processing applications with advanced serial connectivity
- Virtex-5 FXT: Embedded systems with advanced serial connectivity

Virtex-5 LX

Logic Applications

Virtex-5 LX FPGAs are optimized for high performance logic and provide a range of resources and embedded hard IP to facilitate the development of system solutions for the most demanding applications.

<table>
<thead>
<tr>
<th>Resource Type</th>
<th>Resource</th>
<th>LX30</th>
<th>LX50</th>
<th>LX85</th>
<th>LX110</th>
<th>LX220</th>
<th>LX330</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configurable Logic Blocks</td>
<td>CLB Array Size (Row x Column)</td>
<td>80 x 30</td>
<td>120 x 30</td>
<td>120 x 54</td>
<td>160 x 54</td>
<td>160 x 108</td>
<td>240 x 108</td>
</tr>
<tr>
<td></td>
<td>Slices¹</td>
<td>4,800</td>
<td>7,200</td>
<td>12,960</td>
<td>17,280</td>
<td>34,560</td>
<td>51,840</td>
</tr>
<tr>
<td></td>
<td>Logic Cells²</td>
<td>30,720</td>
<td>46,080</td>
<td>82,944</td>
<td>110,592</td>
<td>221,184</td>
<td>331,776</td>
</tr>
<tr>
<td></td>
<td>CLB Flip-Flops</td>
<td>19,200</td>
<td>28,800</td>
<td>51,840</td>
<td>69,120</td>
<td>138,240</td>
<td>207,360</td>
</tr>
<tr>
<td>Memory</td>
<td>Maximum Distributed RMM (Kbits)</td>
<td>320</td>
<td>480</td>
<td>840</td>
<td>1,120</td>
<td>2,280</td>
<td>3,420</td>
</tr>
<tr>
<td></td>
<td>Block RMM/FIFO w/ECC (36Kbits each)</td>
<td>32</td>
<td>48</td>
<td>96</td>
<td>129</td>
<td>192</td>
<td>288</td>
</tr>
<tr>
<td>Clock</td>
<td>Digital Clock Manager</td>
<td>4</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>Phase Locked Loop</td>
<td>2</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>I/O</td>
<td>Maximum SelectIO™ Pins</td>
<td>400</td>
<td>560</td>
<td>560</td>
<td>800</td>
<td>800</td>
<td>1,200</td>
</tr>
<tr>
<td></td>
<td>SelectIO™ Banks</td>
<td>13</td>
<td>17</td>
<td>17</td>
<td>23</td>
<td>23</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>Digitally Controlled Impedance</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>Maximum differential Pairs</td>
<td>200</td>
<td>280</td>
<td>280</td>
<td>400</td>
<td>400</td>
<td>600</td>
</tr>
<tr>
<td>Hard IP</td>
<td>DSP48E Slices</td>
<td>32</td>
<td>48</td>
<td>48</td>
<td>64</td>
<td>128</td>
<td>192</td>
</tr>
<tr>
<td></td>
<td>Configuration Memory (Mbits)</td>
<td>8.4</td>
<td>12.6</td>
<td>21.8</td>
<td>29.1</td>
<td>53.1</td>
<td>79.7</td>
</tr>
</tbody>
</table>

1 - Each Virtex-5 CLB consists of two slices, each with four 6-input look-up tables and four flip-flops for a total of eight 6-input LUTs and eight flip-flops per CLB.
2 - Virtex-5 logic cell ratings reflect the increased logic capacity provided by the new 6-input LUTs

Virtex-5 Features. The XC5VLX110 FPGA is used as standard in VMETRO products.
From Development to Deployment

VMETRO offers system developers the ability to rapidly take advantage of Virtex-5 FPGA performance with a low cost development board in a short PCI card format that can be installed in any standard PC. The card is supplied with a complete software development bundle for the Windows XP operating system that includes:

- VHDL library code blocks (demonstrating how board resources can be used)
- Windows XP drivers
- C support libraries API
- Example code (demonstrating integration of VHDL blocks & library code)
- FLASH programming and board debug utilities
- Hardware and software manuals

Developers can also rapidly deploy a range of PMC based solutions encompassing application areas that require high speed analog input and output, imaging, parallel digital I/O or completely customized I/O.

The product range is based around a common processing node architecture utilizing a Virtex-5 XC5VLX110. The node is equipped with independent banks of fast external memory to support signal processing algorithms: 3 banks of QDR-II SRAM and two banks of DDR2 SDRAM for bulk data storage/buffering. The 256 Mbit Flash memory is large enough to store 3 or more FPGA configuration files. The standard node is also equipped with a 133 MHz PCI-X interface (providing up to 1067 Mbytes/s bandwidth) and 64-bits of user determined rear I/O using Virtex-5 SelectIO™ pins laid out as 32 length-matched differential pairs.

This node commonality means that development work for applications using one member of the board family can be easily transferred to other applications using different signal sources.

Virtex-5 platform Technology Improvements

The Virtex-5 boasts a number of technology advances that enhance embedded reconfigurable processing, including

Signal Processing - 550 MHz DSP48E Slices

Accelerate algorithms and enable higher levels of DSP integration:
- New 25 x 18 multipliers enable single-precision floating point math and wide filters with fewer slices
- Configurable for DSP, arithmetic, and bit-wise logic
- Lower power consumption

Logic Technology

A new architecture using 65nm triple-oxide fabrication technology increases performance:
- Real 6-input Look-Up Tables (LUTs) allow logic to be implemented with fewer logic levels
- Interconnect enables shorter routing for major performance improvements
- 30% higher speed and 35% lower dynamic power than the previous generation

I/O Features

1.25Gbps differential I/O supporting:
- Popular and custom interfaces into the FPGA
- Multiple electrical standards simultaneously at voltages from 1.2V to 3.3V
**Virtex-5 LX FPGA-Products**

### DEV-FPGA05
Low cost PCI/PCI-X development board. Supplied with a complete software development bundle and supports I/O adapter modules for external interfaces (e.g. LVDS).
- Virtex-5 LX110 FPGA
- 138 single-ended (69 differential pairs) I/O lines to front panel I/O module connector
- 64 single-ended I/O lines to rear

### PMC-FPGA05-ADC1
High performance analog to digital conversion via two single ended, AC coupled analog inputs with 50 Ω input impedance.
- 2x 105 MHz, 14-bit ADC
- Virtex-5 LX110 FPGA
- Single-ended, 50 Ω input impedance, AC coupled LVPECL clock input

### PMC-FPGA05-DAC1
High performance digital to analog conversion via two single ended, AC coupled analog outputs.
- 2x 210 MSPS, 14-bit DAC
- Virtex-5 LX110 FPGA
- Single-ended, 50 Ω input impedance, AC coupled LVPECL clock input
**PMC-FPGA05-CAML**

Supports two cameras operating in base mode or one camera in medium or full mode of the Camera-Link specification.
- Up to 85 MHz Camera Link clock rate
- Up to 680 Mbytes/s into FPGA
- Two mini Camera-Link interface connectors

**PMC-FPGA05-FPDPII**

Supports a standard FPDP/FPDP-II interface at the front panel, ideal for direct digital connection to sensor equipment.
- Widely supported data acquisition protocol
- Sustained 400 Mbytes/s bandwidth
- 1067 Mbytes/s PCI-X interface

**PMC-FPGA05-RS422**

Up to 33 Input/Output channel pairs of RS-422B or RS-485 serial interface signaling.
- Virtex-5 LX110 FPGA
- 100 Ω parallel termination and no termination options
- 1067 Mbytes/s PCI-X interface

**PMC-FPGA05-LVDS3**

High performance, low voltage differential signaling (LVDS) front panel I/O
- 32 length matched differential pairs
- 2 independent banks support mixed signaling voltages

**PMC-FPGA05-LRX**

L-Band receiver
- 0.5 to 2 GHz RF Input (+16 to -72dBm)
- Wide-band complex mixer
- Dual 105 MHz 14-bit digitizers
- Automatic Gain Control Input
Application Development Tools

All of VMETRO’s Virtex-5 FPGA products are supported by an extensive package of software libraries, firmware and utilities that aid developers in rapidly exploiting the power of the Virtex-5 family in their applications. Detailed documentation for all hardware, firmware and software features is included with the board support package.

Microsoft Windows XP is the first operating system supported, with WindRiver VxWorks and Linux to follow.

Utilities

To aid application development and debugging, there is a suite of utilities that provide users with tools to:

- Allow Virtex-5 FPGA configurations be written to and read from the board flash
- Allow the FPGA to be rapidly reconfigured from a host or flash file
- Allow registers (including user instantiated registers) and board memory to be visible to a GUI (BView)

Drivers

Initial operating system support is for Windows XP and then VxWorks. The driver permits host applications to reconfigure the Virtex-5 FPGA and provides atomic read/write/modify access to application registers. Read/write access to the flash and read access to I²C sensor registers is also supported.

Versatile interrupt handling, high-performance multi-channel DMA data transfers and built-in test (BIT) are supported. A driver extension framework allows developers to extend the core driver with their own services.

Application Programming Interface

An API provides programmers with access to the board hardware/firmware modules through extensive task/thread safe C libraries. They allow developers to quickly take advantage of powerful board features in their applications, including the PCI-X interface DMA engines and interrupt handlers.

Numerous examples accompany the BSP which demonstrate the correct use of each major area of API functionality, allowing programmers to ‘hit the ground running’ when using library functionality in real-world applications.

Built-in test (BIT) tools are also provided allowing the developer or their application to ascertain the operational condition of the board’s hardware features.
Firmware

All interfaces between the Virtex-5 FPGA and external devices are supported by firmware which is supplied as IP to users. Each IP block has standardized back end interfaces, allowing developers to quickly integrate their own custom logic (for example, signal processing algorithms) or commercial third party IP to the hardware interfaces of the board (for example the external memory interfaces or an I/O mechanism). The firmware also provides a start point for developers to create customized hardware operation.

Toolchain Support

The firmware supplied in the BSP is created using the latest version of Xilinx Foundation™.
**Product Range**

VMETRO’s Virtex-5 FPGA boards are available with a broad selection of I/O choices. Boards are also available without dedicated front panel I/O allowing developers to create custom I/O solutions tailored to their application. The table below gives a brief summary of the resources available to each Virtex-5 board. For more detailed information about these products, please visit the VMETRO website where datasheets are available for download. Alternatively, please contact your VMETRO representative.

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Type</th>
<th>FPGA</th>
<th>Primary I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV-FPGA05</td>
<td>PCI</td>
<td>LX110</td>
<td>Front panel module I/O</td>
</tr>
<tr>
<td>PMC-FPGA05</td>
<td>PMC</td>
<td>LX110</td>
<td>138-bit customizable I/O</td>
</tr>
<tr>
<td>PMC-FPGA05-RDC1</td>
<td>PMC</td>
<td>LX110</td>
<td>2x 14-bit 105MHz ADCs</td>
</tr>
<tr>
<td>PMC-FPGA05-DAC1</td>
<td>PMC</td>
<td>LX110</td>
<td>2x 14-bit 210MHz DACs</td>
</tr>
<tr>
<td>PMC-FPGA05-LVDS3</td>
<td>PMC</td>
<td>LX110</td>
<td>32-pair LVDS I/O</td>
</tr>
<tr>
<td>PMC-FPGA05-CAML</td>
<td>PMC</td>
<td>LX110</td>
<td>Base or medium/full Camera Link input</td>
</tr>
<tr>
<td>PMC-FPGA05-FPDII</td>
<td>PMC</td>
<td>LX110</td>
<td>FPDP/FPDP-II</td>
</tr>
<tr>
<td>PMC-FPGA05-RS422</td>
<td>PMC</td>
<td>LX110</td>
<td>33 channel 422/485</td>
</tr>
<tr>
<td>PMC-FPGA05-LRX</td>
<td>PMC</td>
<td>LX110</td>
<td>L-band Receiver</td>
</tr>
</tbody>
</table>

Please contact your VMETRO representative for more information or a product demonstration.