

General Standards Corporation

High Performance Bus Interface Solutions

12AISS44AO4

12-Channel, 12-Bit PMC Analog Input/Output Board

With Eight Simultaneously-Sampled Wide-Range Inputs at 2.0 MSPS per Channel,
Four Analog Outputs, and 16-Bit Digital I/O Port

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

PMC-12AISS44AO4:	PMC, Single-width
PCI-12AISS44AO4:	PCI, short length
cPCI-12AISS44AO4:	cPCI, 3U
PC104P-12AISS44AO4:	PC104-Plus
PCIe-12AISS44AO4:	PCI Express
PCIe104-12AISS44AO4:	PCIe, one-lane on PC/104 form factor

See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

FEATURES

- ♦ **8 Differential Analog Inputs with Dedicated 12-Bit, 2.0 MSPS ADC per Channel**
 - ♦ True Simultaneous Sampling of all Inputs; Minimum Data Skew
 - ♦ Sampling Rates to 2.0 MSPS per Channel (16 MSPS Aggregate Rate)
 - ♦ Two Input Range Groups; Each Factory Configured as $\pm 100\text{mV}$, $\pm 1\text{V}$ or $\pm 10\text{V}$
 - ♦ 64-Ksample Analog Input FIFO Data Buffer
 - ♦ Supports Two DMA Channels in Block-Mode or Demand-Mode
- ♦ **4 Analog Output Channels with Direct Register Access**
- ♦ **16-Bit Bidirectional Digital I/O Port**
- ♦ Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- ♦ On-Demand Internal Autocalibration
- ♦ Hardware Sync I/O for Multiboard Operation
- ♦ Full Power Bandwidth to 900kHz at 4Vp-p; to 220kHz at 20Vp-p
- ♦ Conforms to PCI Local Bus Specification, Revision 2.3, with Universal Signaling
- ♦ Single-width PMC Form Factor

APPLICATIONS

- Wideband Analog Inputs
- Transducer Inputs
- Dynamic Test Systems
- Low-Level Inputs
- Event Capture
- Voltage Control
- Instrumentation
- Acoustic Sensor Inputs
- Closed-Loop Systems

Rev: 080510

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FUNCTIONAL DESCRIPTION

The 12-Bit PMC-12AISS44AO4 analog I/O board samples and digitizes eight input channels simultaneously at rates up to 2.0 million samples per second for each channel. 12-bit sampled data is available to the PCI bus through a 64K-Sample FIFO buffer. All data is channel-tagged.

Analog input sampling can be controlled from an internal rate generator, through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are factory-configured as $\pm 1V$, $\pm 100mV$ or $\pm 10V$ for each of two input channel groups.

Four analog output channels provide software-selected output ranges of $\pm 2.5V$, $\pm 5V$ or $\pm 10V$, and are accessed directly through dedicated control registers. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

An on-demand autocalibration feature determines offset and gain correction values for each input and output channel, and the corrections are applied subsequently during normal operation. A selftest switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host..

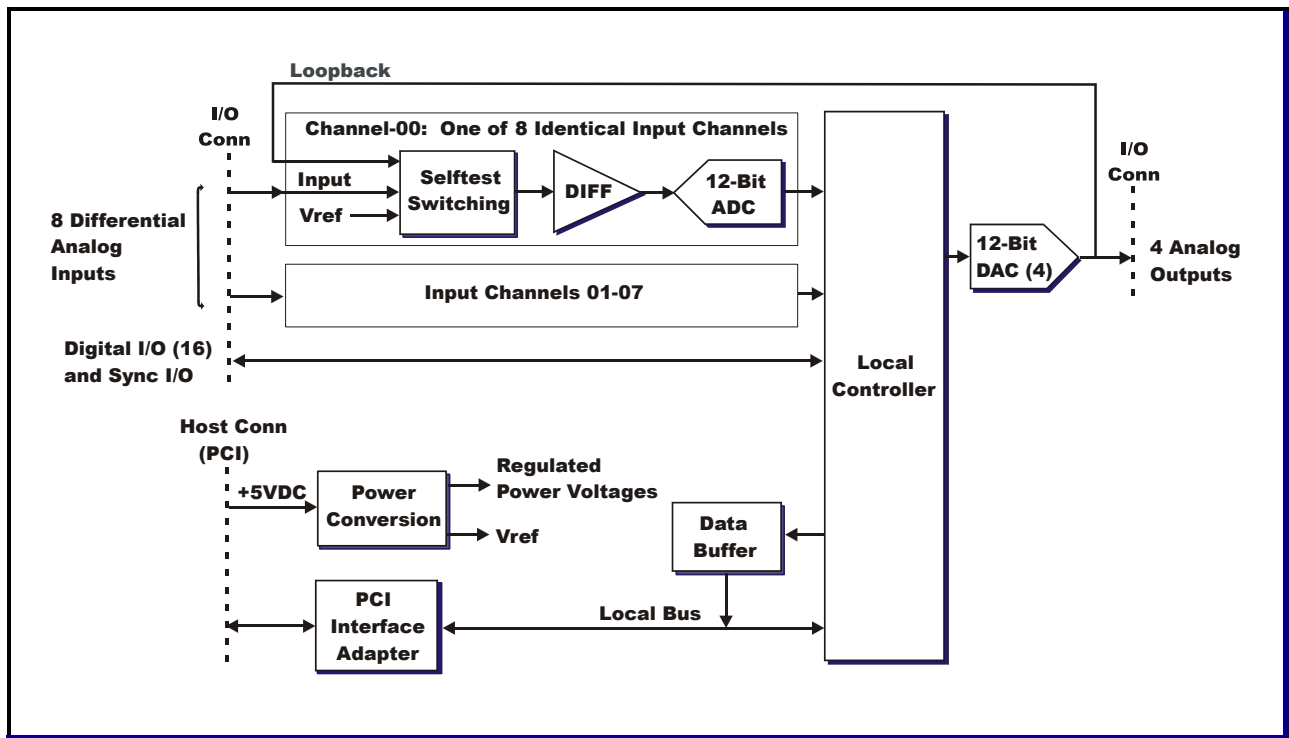


Figure 1. PMC-12AISS44AO4; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional convection cooling.

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PERFORMANCE SPECIFICATIONS

At +25 °C, with specified operating voltages

Analog Input Characteristics:

Configuration:	Eight differential analog input channels; Dedicated 12-Bit ADC per channel. Optional 4-Channel version available.
Voltage Ranges:	Two channel groups, each factory configured as $\pm 100\text{mV}$, $\pm 1\text{V}$ or $\pm 10\text{V}$ fullscale.
Input Impedance:	20 Megohms Line-Line in parallel with 40pF, typical.
Bias Current:	50 nanoamps maximum, all ranges.
Crosstalk Rejection:	70dB typical, DC-500kHz.
Signal/Noise Ratio (SNR):	$\pm 1\text{V}$, $\pm 10\text{V}$ Ranges: 70dB, $\pm 100\text{mV}$ Range: 65dB; typical. (10 Hz to specified small-signal bandwidth. Signal = Fullscale-0.3dB).
Common Mode Rejection:	$\pm 1\text{V}$, $\pm 10\text{V}$ Ranges: 85dB, $\pm 100\text{mV}$ Range: 95dB. Typical, DC-100Hz, CMV = $\pm 11\text{V}$, V_{in} = Zero.
Oversvoltage Protection:	± 40 Volts with power removed; $\pm 25\text{V}$ with power applied.

Analog Input Transfer Characteristics:

Resolution:	12 Bits (0.0244 percent of FSR).												
Maximum Sample Rate:	2.0 MSPS per channel.												
Sampling Mode:	Simultaneous; 1 through 8 channels.												
DC Accuracy: (Maximum composite error after autocalibration)	<table><thead><tr><th>Range</th><th>Midscale Accuracy</th><th>Fullscale Accuracy</th></tr></thead><tbody><tr><td>$\pm 10\text{V}$</td><td>$\pm 7\text{ mV}$</td><td>$\pm 25\text{mV}$</td></tr><tr><td>$\pm 1\text{V}$</td><td>$\pm 2\text{ mV}$</td><td>$\pm 8\text{mV}$</td></tr><tr><td>$\pm 100\text{mV}$</td><td>$\pm 1\text{ mV}$</td><td>$\pm 3\text{mV}$</td></tr></tbody></table>	Range	Midscale Accuracy	Fullscale Accuracy	$\pm 10\text{V}$	$\pm 7\text{ mV}$	$\pm 25\text{mV}$	$\pm 1\text{V}$	$\pm 2\text{ mV}$	$\pm 8\text{mV}$	$\pm 100\text{mV}$	$\pm 1\text{ mV}$	$\pm 3\text{mV}$
Range	Midscale Accuracy	Fullscale Accuracy											
$\pm 10\text{V}$	$\pm 7\text{ mV}$	$\pm 25\text{mV}$											
$\pm 1\text{V}$	$\pm 2\text{ mV}$	$\pm 8\text{mV}$											
$\pm 100\text{mV}$	$\pm 1\text{ mV}$	$\pm 3\text{mV}$											
Small-Signal Bandwidth:	DC to 900kHz, all ranges. 3dB typical.												
Settling Time (0.01%):	2.3 μs , all ranges, typical												
Power Bandwidth; -3dB	900kHz from 0Vp-p to 4Vp-p. 220kHz at 20Vp-p. 3dB typical.												
Integral Nonlinearity:	± 0.035 percent FSR.												
Differential Nonlinearity:	± 0.030 percent FSR.												

Analog Input Operating Modes and Controls

Input Data Buffer:	64K-sample FIFO.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generator:	Programmable from 488-2,000,000 sample clocks per second. Divides 32MHz master clock to sample rate.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.
Input Data Format:	Selectable as offset binary or as two's complement. All channels tagged.

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Analog Output Characteristics:

Configuration:	Four single-ended output channels.
Voltage Ranges:	± 10 , ± 5 or ± 2.5 Volts; Software-selectable; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum.
Output protection:	Withstands sustained short-circuiting to ground.
Load Current:	Zero to ± 5 ma per channel.
Load Capacitance:	Stable with any load capacitance.
Noise:	2.0mV-RMS, 10Hz-100KHz typical.
Glitch Impulse:	5 LSB-nSec typical, all ranges.

Analog Output Transfer Characteristics:

Resolution:	12 Bits (0.0244 percent of FSR)		
Output Clocking:	Direct register access. Outputs can update immediately upon receiving each new value from the bus, or can update synchronously from an internal or external clock. Maximum practical clocking rate is 400KSPS per channel.		
DC Accuracy: (Max error, no-load)	<u>Range</u>	<u>Midscale Accuracy</u>	<u>\pmFullscale Accuracy</u>
	± 10 V	± 10 mV	± 35 mV
	± 5 V	± 4 mV	± 18 mV
	± 2.5 V	± 2 mV	± 10 mV
Settling Time:	4us to 1-LSB, typical with 50-percent fullscale step, no-load.		
Crosstalk Rejection:	65 dB minimum, DC-10 kHz.		
Integral Nonlinearity:	± 0.04 percent of FSR, maximum.		
Differential Nonlinearity:	± 0.03 percent of FSR, maximum.		

Digital I/O Port:

16-Bit bidirectional I/O port. Standard TTL levels. Direct register Access. Byte or word configuration. 20 mA loading when configured as an output port. 0.1 mA source when configured as inputs.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33MHz, universal (5V/3.3V) signaling,
Supports "plug-n-play" initialization,
Provides one multifunction interrupt,
Supports DMA data transfers in two channels as bus master in block mode or demand mode.

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ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number PMC-12AISS44AO4-8-64K-4-LH describes a board with eight input channels, four output channels, a 64 Ksample data buffer, four $\pm 100\text{mV}$ inputs and four $\pm 1\text{V}$ inputs.

Basic Model Number	Form Factor
PMC-12AISS44AO4	PMC (Native)
PCI-12AISS44AO4¹	PCI, short length
cPCI-12AISS44AO4¹	cPCI, 3U
PCle-12AISS44AO4¹	cPCI, 3U
PC104P-12AISS44AO4	PC104-Plus
PCle104-12AISS44AO4^{1,2}	PCle, one-lane on PC/104 form factor

¹ Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

² PCle104 supports only the PCle bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	8 Input Channels	A = 8
	4 Input Channels	A = 4
Buffer Size	64 Ksamples	B = 64K
Analog Outputs	Four Analog Outputs	C = 4
	No Analog Outputs	C = 0
Input Ranges	Group-A and Group-B = $\pm 100\text{mV}$	D=LL
	Group-A = $\pm 100\text{mV}$; Group-B = $\pm 1\text{V}$	D=LH
	Group-A and Group-B = $\pm 1\text{V}$	D=HH
	Group-A = $\pm 100\text{mV}$; Group-B = $\pm 10\text{V}$	D=LV
	Group-A = $\pm 10\text{V}$; Group-B = $\pm 10\text{V}$	D=VV

General Standards Corporation assumes no responsibility for the use of any circuits in this product. No circuit patent licenses are implied. Information included herein supersedes previously published specifications on this product and is subject to change without notice.

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SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	OUTPUT RTN	1	DIGITAL RTN
2	ANA OUT 00	2	DIO 00
3	OUTPUT RTN	3	DIGITAL RTN
4	ANA OUT 01	4	DIO 01
5	OUTPUT RTN	5	DIGITAL RTN
6	ANA OUT 02	6	DIO 02
7	OUTPUT RTN	7	DIGITAL RTN
8	ANA OUT 03	8	DIO 03
9	INPUT RTN	9	DIGITAL RTN
10	INPUT RTN	10	DIO 04
11	INP00 LO *	11	DIGITAL RTN
12	INP00 HI *	12	DIO 05
13	INPUT RTN	13	DIGITAL RTN
14	INPUT RTN	14	DIO 06
15	INP01 LO *	15	DIGITAL RTN
16	INP01 HI *	16	DIO 07
17	INPUT RTN	17	DIGITAL RTN
18	INPUT RTN	18	DIO 08
19	INP02 LO **	19	DIGITAL RTN
20	INP02 HI **	20	DIO 09
21	INPUT RTN	21	DIGITAL RTN
22	INPUT RTN	22	DIO 10
23	INP03 LO **	23	DIGITAL RTN
24	INP03 HI **	24	DIO 11
25	INPUT RTN	25	DIGITAL RTN
26	INPUT RTN	26	DIO 12
27	INP04 LO *	27	DIGITAL RTN
28	INP04 HI *	28	DIO 13
29	INPUT RTN	29	DIGITAL RTN
30	INPUT RTN	30	DIO 14
31	INP05 LO *	31	DIGITAL RTN
32	INP05 HI *	32	DIO 15
33	INPUT RTN	33	VTEST RTN
34	INPUT RTN	34	VTEST
35	INP06 LO **	35	DIGITAL RTN
36	INP06 HI **	36	OUTPUT CLK I/O
37	INPUT RTN	37	DIGITAL RTN
38	INPUT RTN	38	INPUT TRIG I/O
39	INP07 LO **	39	DIGITAL RTN
40	INP07 HI **	40	INPUT CLK I/O

* Input Group-A. ** Input Group-B.

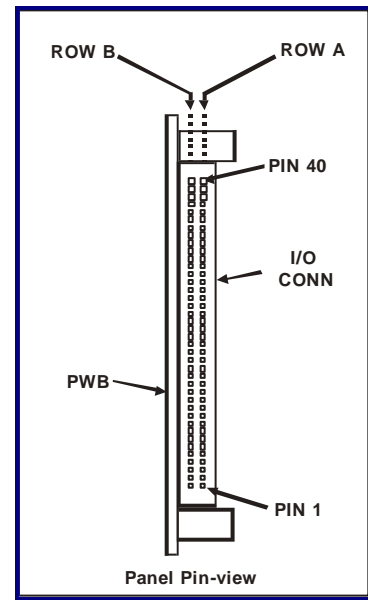


Figure 2. System Input Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent P50E-080S-TG, or equivalent.

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