

General Standards Corporation

High Performance Bus Interface Solutions

14HSAI4

14-Bit, 4-Channel, 50MSPS/Channel PMC Analog Input Board

With 66MHz PCI Compatibility, Multiple Ranges, and Data Packing

Available in PMC, PCI, cPCI and PC104-Plus and PCI Express form factors as:

PMC66-14HSAI4:	PMC, Single-width
PCI66-14HSAI4:	PCI, short length
cPCI66-14HSAI4:	cPCI, 3U
PC104P66-14HSAI4:	PC104-Plus
PCIe-14HSAI4:	PCI Express
PCIe104-14HSAI4:	PCIe, one-lane on PC/104 form factor

See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

FEATURES:

- ♦ **Four-Channel, 14-Bit Wideband Analog Input Board**
- ♦ **Sampling Rates to 50 MSPS per Channel**
- ♦ **Sustainable Aggregate Conversion Rates to 100 MSPS**
- ♦ **Four Wideband Analog Inputs with a Dedicated 14-Bit ADC per Channel**
- ♦ **Software-Selectable Input Ranges: $\pm 10V$, $\pm 5V$, $\pm 2.5V$.**
- ♦ **Optional Input Ranges: $\pm 2.5V$, $\pm 1.25V$, $\pm 0.625V$, or Transformer-Coupled 2Vp-p, 1Vp-p**
- ♦ **DC Accuracy as well as AC performance**
- ♦ **1-MByte FIFO Data Buffer**
- ♦ **66MHz PCI Compatibility and DMA Engine Provide Maximum Throughput**
- ♦ **Sync-on-Level and Pretrigger Oscilloscope Triggering Functions**
- ♦ **Software-Configurable Data Path Supports Data Packing**
- ♦ **Both Coaxial and Ribbon-Cable System Connections are Supported**
- ♦ **Simultaneous Sampling of All Channels**
- ♦ **Sample Clocking Supplied by Internal Rate Generator or External Source**
- ♦ **Hardware Sync I/O for Multiboard Synchronization**
- ♦ **On-Demand Internal Autocalibration in High-Level and Wideband Configurations**
- ♦ **Conforms to PCI Local Bus Specification, Revision 2.3, with Universal Signaling**
- ♦ **Single-width PMC Form Factor with Integral EMI Shield**

TYPICAL APPLICATIONS

- Wideband Analog Inputs
- Event Capture
- Imaging Systems
- Telecommunications
- Spectrum Analysis
- Dynamic Test Systems

Rev: 080510

Functional Description

The 14-Bit PMC66-14HSAI4 analog input board samples and digitizes as many as four analog input channels simultaneously at sustainable aggregate rates up to 100 million conversions per second. Each input channel implements a dedicated 14-Bit ADC for data conversion, and the resulting 14-bit sampled data is available to the PCI bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing, and data throughput is further enhanced with 66MHz PCI support. The sample clock can be generated from an internal rate generator or by external hardware, and multiple boards can be operated synchronously. Pretrigger and Sync-on-Level oscilloscope burst-triggering functions are supported. All operational parameters are software configurable.

Input ranges are software-selectable as $\pm 2.5V$, $\pm 1.25V$ or $\pm 0.625V$ for the standard Wideband input configuration. Input range options also include a High-Level configuration with selectable ranges of $\pm 10V$, $\pm 5V$ or $\pm 2.5V$, and a Transformer-Coupled configuration with 2Vp-p and 1Vp-p ranges. Wideband and Hi-Level inputs are DC-coupled; Transformer-Coupled inputs are AC-coupled. The analog inputs can be jumper-configured as either differential or single-ended.

For the Wideband and High-Level input configurations, on-demand autocalibration determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

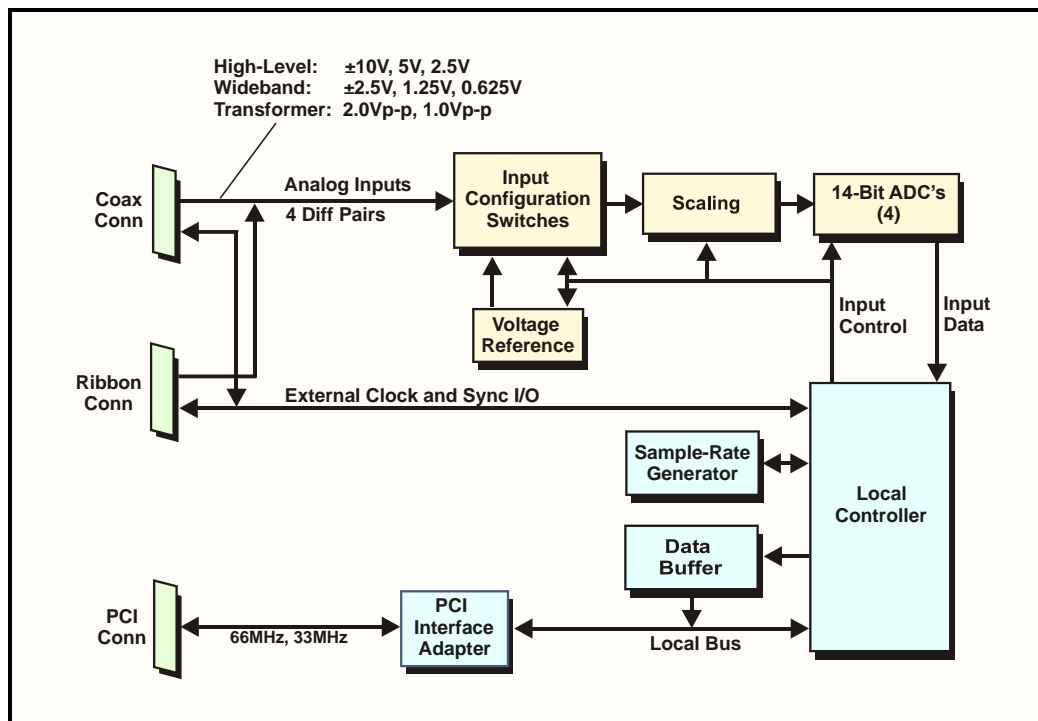


Figure 1. PMC66-14HSAI4; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel, either through standard MMCX coaxial connectors or through a high-density ribbon-cable connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional PMC cooling.

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Performance Specifications

At +25 °C, with specified operating conditions

Input Characteristics:

Configuration:	Four differential input channels, jumper-configurable as single-ended*. Dedicated 14-Bit ADC per channel. Optional two-channel version available.
Input Voltage Ranges:	High-Level: $\pm 10V$, $\pm 5V$, $\pm 2.5V$. Wideband: $\pm 2.5V$, $\pm 1.25V$, $\pm 0.625V$. Transformer: 2.0Vp-p, 1.0Vp-p.
Input Impedance, Typical, line-line:	High-Level: 2 Megohms in parallel with 25pFd. Wideband: 2 Megohms in parallel with 12 pFd. Optional 50-Ohms. Transformer: 50-Ohms in parallel with 12 pFd.
Common Mode Voltage; (CMV; Zero signal):	High-Level: $\pm 11 V$. Wideband: $\pm 3.5 V$. Transformer: $\pm 75V$ (Galvanically isolated from the PCI bus).
Input Protection, Sustained Overvoltage:	Line-Line (Differential inputs only. Single-ended inputs same as Line-Ground): High-Level: ± 30 Volts with power applied; $\pm 6V$ with power removed. Wideband: ± 10 Volts with power applied; $\pm 4V$ with power removed; 3.5Vrms with 50-Ohm input option. Transformer: 3Vp-p or $\pm 40VDC$; power applied or removed. Line-Ground: High-Level#: ± 16 Volts with power applied; $\pm 3V$ with power removed. Wideband#: ± 6 Volts with power applied; $\pm 2V$ with power removed. Transformer: $\pm 100VDC$; with power applied or removed.

* Single-ended inputs have "LO" inputs internally connected to system ground. Common-mode characteristics apply only to differential inputs.

Transfer Characteristics:

Resolution:	14 Bits (0.0061 percent of FSR)																		
Effective Sample Rate:	Sustainable 1 KSPS to 50 MSPS per channel for two active channels in packed data mode; 25MSPS per channel for four channels. Sustainable aggregate rates to 100 MSPS.																		
Input Bandwidth:	High-Level: DC-25MHz (-3dB), 0.1dB at 3 MHz. Wideband: DC-65MHz (-3dB), 0.1dB at 12 MHz. Transformer: 0.7-130 MHz (-3dB); $\pm 1dB$ accuracy at 5MHz.																		
Power Bandwidth:	200 MHz-Vpp for the Wideband and Transformer configurations. (e.g.: 10Vp-p at 20MHz). 50 MHz-Vpp for the High-Level configuration.																		
DC Accuracy *:	<table><thead><tr><th>Range</th><th>Zero-Input</th><th>Fullscale</th></tr></thead><tbody><tr><td>$\pm 10V$</td><td>$\pm 5mv$</td><td>$\pm 11mv$</td></tr><tr><td>$\pm 5V$</td><td>$\pm 3mv$</td><td>$\pm 6mv$</td></tr><tr><td>$\pm 2.5V$</td><td>$\pm 2mv$</td><td>$\pm 4mv$</td></tr><tr><td>$\pm 1.25V$</td><td>$\pm 2mv$</td><td>$\pm 3mv$</td></tr><tr><td>$\pm 0.625V$</td><td>$\pm 1mv$</td><td>$\pm 2mv$</td></tr></tbody></table>	Range	Zero-Input	Fullscale	$\pm 10V$	$\pm 5mv$	$\pm 11mv$	$\pm 5V$	$\pm 3mv$	$\pm 6mv$	$\pm 2.5V$	$\pm 2mv$	$\pm 4mv$	$\pm 1.25V$	$\pm 2mv$	$\pm 3mv$	$\pm 0.625V$	$\pm 1mv$	$\pm 2mv$
Range	Zero-Input	Fullscale																	
$\pm 10V$	$\pm 5mv$	$\pm 11mv$																	
$\pm 5V$	$\pm 3mv$	$\pm 6mv$																	
$\pm 2.5V$	$\pm 2mv$	$\pm 4mv$																	
$\pm 1.25V$	$\pm 2mv$	$\pm 3mv$																	
$\pm 0.625V$	$\pm 1mv$	$\pm 2mv$																	
Signal to Noise (SNR):	$\pm 10V$ Range, 67dB; $\pm 5V$ Range, 65dB; $\pm 2.5V$ Range, 60dB; $\pm 1.25V$ Range: 57dB; $\pm 0.625V$ Range: 55dB. Typical at 25MSPS, with $V_{sig} = V_{fs-rms}$.																		
Crosstalk Rejection:	80dB minimum at 10MHz, all ranges																		

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Transfer Characteristics (Continued):

Harmonic Distortion (THD):	-90dB to 1MHz; -50dB to 20MHz. 0.4FSR; Hi-Level and Wideband.
Common Mode Rejection (CMRR, typical):	High-Level: 40dB, DC to 3MHz. Wideband: 40dB, DC to 10MHz. Transformer: 40dB, DC to 15MHz.
Integral Nonlinearity *:	±0.02 percent of FSR, maximum
Differential Nonlinearity *:	±0.006 percent of FSR, maximum

* High-Level and Wideband configurations. 50-Ohm input termination resistors will increase the maximum fullscale errors to ±3%

Operating Modes and Controls

Input Data Buffer:	1 MByte; 512 K-Samples in packed-data mode.
Sample Clock Sources:	Internal rate generator or external hardware I/O.
Rate Generator:	Programmable from 1-50 million sample clocks per second with 0.03-percent accuracy. Lower effective sample rates down to 1KSPS are obtained by simple decimation.
External Sync I/O:	Bidirectional clock or trigger (sync) I/O; 1-50MHz for sample clocking. Burst triggering from 0-5MHz as a sync target input, or 24Hz - 5MHz as an initiator output.. TTL through coaxial connectors; differential (LVDS) through the ribbon-cable connector.
Input Data Format:	Nonpacked Mode: 14-Bit data plus channel tag. Packed Mode: Consecutive channel samples occupy lower and upper 16-Bit fields in a 32-Bit Longword.
Data Format:	Selectable as offset binary or two's complement.
Pretriggering:	A selectable number of pretrigger-samples is acquired immediately prior to a burst trigger.
Sync-on-Level:	Sync (burst-trigger) is generated from a selectable input level in any input channel. Selectable filtering (integration) and holdoff functions

PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 data, and universal signaling (5/3.3 Volt). DMA block-mode transfers as bus master. Two DMA channels available.

Power Requirements

+5VDC ±0.2 VDC at 1.5 Amps maximum, 1.2 Amps typical.

Typical Power Dissipation: Side-1: 4.5 Watts. Side 2: 1.5 Watts.

Physical Parameters

Mechanical Characteristics (PMC Form Factor)

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side-1 is protected by an EMI shield.

* Mechanical dimensions are shown for the native PMC form factor. See Ordering Information.

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Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +60 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number PMC66-14HSAI4-4-HL-2M describes a PMC module with four high-level differential input channels and a 2-Megohm input impedance.

Basic Model Number	Form Factor
PMC66-14HSAI4	PMC (Native)
PCI66-14HSAI4 ¹	PCI, short length
CPCI66-14HSAI4 ¹	cPCI, 3U
PCle-14HSAI4 ¹	cPCI, 3U
PC104P66-14HSAI4	PC104-Plus
PCle104-14HSAI4 ^{1,2}	PCle, one-lane on PC/104 form factor

¹ Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

² PCle104 supports only the PCle bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Channels	A = 4
	2 Channels	A = 2
Input Configuration *	High-Level ($\pm 10V$, $\pm 5V$, $\pm 2.5V$)	B = HL
	Wideband ($\pm 2.5V$, $\pm 1.25V$, ± 0.625)	B = WB
	Transformer (2Vp-p, $\pm 1Vp-p$)	B = TR
Input Impedance	2 Megohms **	C = 2M
	50 Ohms *** (Required for transformer inputs)	C = 50
Custom Feature	No custom feature	D = 0 or blank
	Omit FP-P1 I/O Connector	D = P1

* Refer to Input Characteristics and Transfer Characteristics for associated performance parameters such as bandwidth and SNR.

** High-Level and Wideband input configurations only.

*** Wideband and Transformer input configurations only.

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Table 1. System Ribbon-Cable Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INPUT RETURN	1	INPUT RETURN
2	INPUT 00 HI	2	INPUT 03 HI
3	INPUT 00 LO	3	INPUT 03 LO
4	INPUT RETURN	4	INPUT RETURN
5	INPUT 01 HI	5	DIGITAL RETURN
6	INPUT 01 LO	6	SYNC I/O HI
7	INPUT RETURN	7	SYNC I/O LO
8	INPUT 02 HI	8	DIGITAL RETURN
9	INPUT 02 LO	9	CLOCK I/O HI
10	INPUT RETURN	10	CLOCK I/O LO

System Mating Connectors:

FP-J1 Thru J6: Standard MMCX Coax cable plug:
 Examples: (Straight cable plug;
 crimp or solder):
 Johnson 135-3403-001 (RG-316),
 Johnson 135-3402-001 (RG-178).

FP-P1: High-Density 20-Pin 0.050-inch socket:
 Robinson-Nugent P50E-020S-TG,
 or equivalent.
 (Board connector: P50E-020P1-SR1-TG)

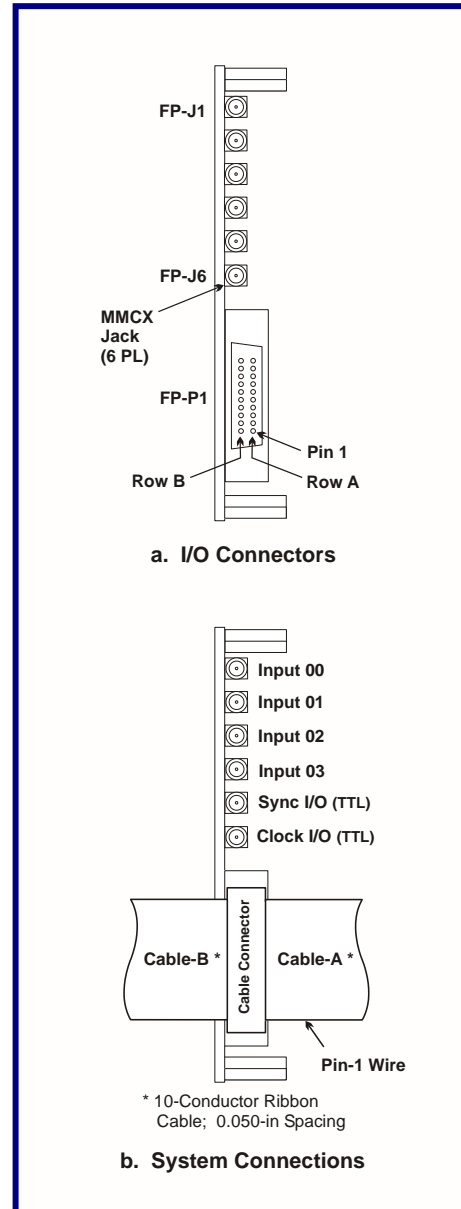


Figure 2. System I/O

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