General Standards Corporation

High Performance Bus Interface Solutions

16AIO168

16-Bit Analog Input/Output Board

With 16 Input Channels and 8 Output Channels

Available in PMC, PCI, cPCI, PCI-104 and PC104-*Plus* and PCI Express form factors as:

PMC-16AIO168:	**PMC**, Single-width
PCI-16AIO168:	**PCI**, short length
cPCI-16AIO168:	**cPCI,** 3U
PC104P-16AIO168:	**PC104-*Plus***
PCI104-16AIO168:	**PCI-104**; No ISA passthrough
PCIe-16AIO168:	**PCI Express**, short length
PCIe104-16AIO168:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details.
Call for availability of other form factors, such as XMC, CCPMC, etc.

Features Include:

- 16 Single-Ended or 8 Differential 16-Bit Scanned Analog Input Channels
- Eight Analog Output Channels, 16-Bit D/A Converter per Channel
- Software-Selectable Analog Input/Output Ranges of ±10V, ±5V or ±2.5V
- Independent 32K-Sample Analog Input and Output FIFO Buffers
- 300K Samples per Second Aggregate Analog Input Sample Rate
- Multiple-Channel and Single-Channel Input Scanning Modes
- Low Crosstalk, Noise and Input Bias Current; Buffer Amplifiers on all Analog Input Lines
- 300K Samples per Second per Channel Analog Output Clocking Rate
- Supports Waveform and Arbitrary Function Generation; Continuous and One-shot Modes
- Internal Rate Generator Controls Input Sampling, Output Sampling, or Both Simultaneously
- Supports Multiboard Synchronization of Analog Inputs and Outputs
- Four Auxiliary Digital Output Lines
- Internal Auto calibration of Analog Input and Output Channels
- Continuous and Burst (One-Shot) Input and Output Modes
- DMA Engine Minimizes Host I/O Overhead

Applications:

- ❑ Data Acquisition Systems
- ❑ Industrial Robotics
- ❑ Precision Voltage Sourcing and Measurement
- ❑ Automatic Test Equipment
- ❑ Function and Waveform Generation
- ❑ Research Instrumentation

Rev: 072114

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Functional Description:

The 16AIO168 board provides high-speed 16-bit analog input/output resources in a standard form-factor I/O module. Eight analog output channels can be updated either synchronously or asynchronously, and support waveform generation. Each analog output channel contains a dedicated 16-bit D/A converter and an output range control network. The board receives analog output data from the PCI bus through a 32K-sample FIFO buffer.

The analog inputs are software-configurable either as 16 single-ended channels or as eight differential signal pairs. Buffer amplifiers on all input lines eliminate multiplexer input switching noise, and minimize crosstalk and input bias currents. Analog input data accumulates in a 32K-sample buffer until retrieved through the PCI bus.

Internal autocalibration networks permit the calibration of all analog input and output channels without removing the board from the system. Gain and offset corrections of the analog input and output channels are performed by calibration DAC's that are loaded with channel correction values during autocalibration. Software-controlled test configurations include a loopback mode for monitoring any analog output channel. Trigger input and output connections support external triggering and multiboard synchronization.

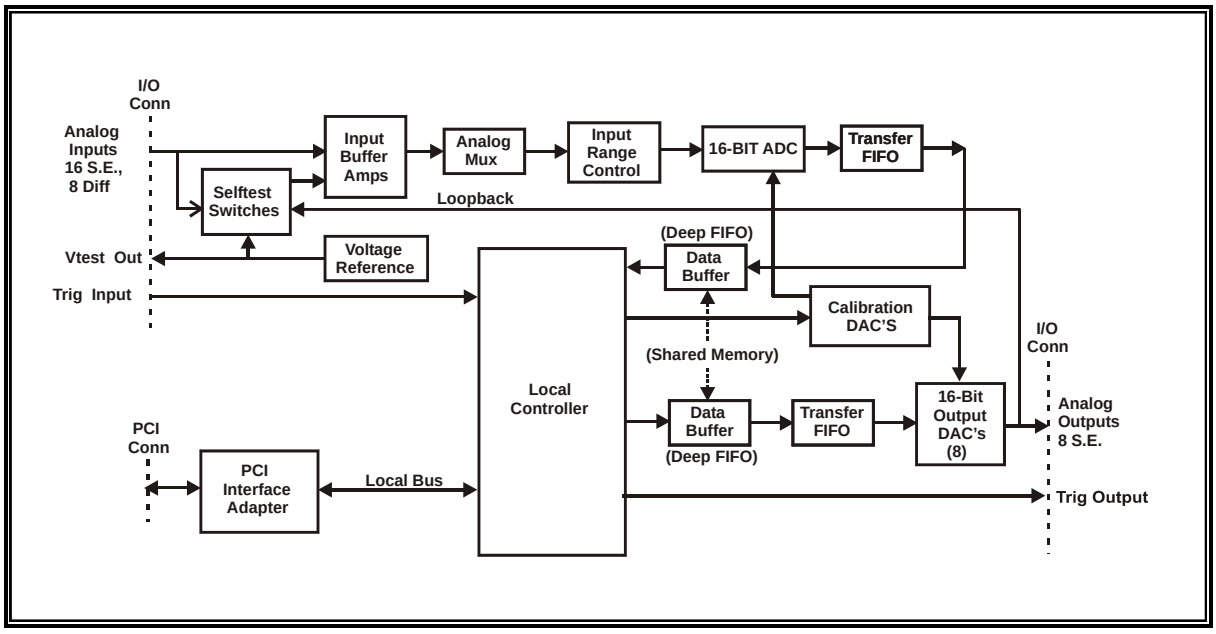

Figure 1. 16AIO168; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and the PC104-*Plus* Specification Version 1.1 if applicable. System input/output connections are made through a either a standard 50-pin I/O connector, or a SCSI-3 I/O connector (See ordering options). Operation over the specified temperature range is achieved with conventional convection cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

ANALOG INPUT CHANNELS

❑ Input Characteristics:

Configuration:	16 input lines, configurable as 16 single-ended or 8 differential channels
Voltage Ranges:	Software configurable as ±10, ±5 or ±2.5 Volts
Input Impedance:	1.0 Megohms line-to-ground, 2.0 Megohms line-to-line, in parallel with 100Pfd. Independent of scan rate.
Bias Current:	80 nanoamps maximum
Noise:	2.0 LSB-RMS typical
Common Mode Rejection:	60 dB typical, DC-60 Hz, differential input mode
Common Mode Range:	±10 Volts; differential input configuration
Overvoltage Protection:	Standard: ±30 Volts with power applied; ±15 Volts with power removed

❑ Transfer Characteristics:

Resolution:	16 Bits; 0.0015 percent of FSR
Maximum Conversion Rate:	300K conversions per second, minimum
Channels per scan:	1, 2, 4, 8, or 16 Channels per scan (16 channels available only in single-ended mode)
Maximum Scan Rate:	150 KSPS in multiple-channel scanning mode. 300KSPS in single-channel mode. Scan rate equals the conversion rate divided by the number of channels per scan.
Minimum Scan Rate:	460 scans per second, using a single internal rate generator; 0.007SPS using both generators. Zero, using a software sync flag or an externally supplied sync input.

DC Accuracy (Maximum composite error, referred to inputs):

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±3.2mV	±4.2mV
±5V	±2.3mV	±2.8mV
±2.5V	±1.6mV	±2.0mV

Crosstalk Rejection:	85dB, DC-10kHz
Integral Nonlinearity:	±0.003 percent of FSR, maximum
Differential Nonlinearity:	±0.0015 percent of FSR, maximum

❑ Analog Input Operating Modes and Controls

Analog Input Modes:	Single Scan:	Software or hardware trigger initiates a single scan of all active channels at the maximum conversion rate.
	Continuous Scan:	Inputs are scanned continuously at the selected scan rate.
	Selftest:	Reference and loopback tests; autocalibration
	Multiple-Channel:	2, 4, 8, 16 channels per scan (Includes 2-Channel mode).
	Single-Channel:	Any single channel can be selected for digitizing at the maximum conversion rate.
Input Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported	

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ANALOG OUTPUT CHANNELS

Output Characteristics:

Configuration:	Eight single-ended output channels. (Ordering option)
Voltage Ranges:	Same as selected for analog inputs; ±10, ±5 or ±2.5 Volts
Output Resistance:	1.0 Ohm, maximum
Output protection:	Withstands sustained short-circuit to output return
Load Current:	Zero to ±5ma per individual channel; maximum total of 30ma total for all channels.
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	5 nV-Sec typical, ±2.5V range

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Output Sample Rate:	Software adjustable from 400SPS to 300KSPS per channel; 0.006SPS to 300KSPS using both internal rate generators. DC to 300KSPS with hardware or software sync.

DC Accuracy: (Maximum composite error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±2.7mV	±3.0mV
±5V	±1.9mV	±2.2mV
±2.5V	±1.3mV	±1.7mV

Settling Time:	8us to 1LSB, typical with 50-percent fullscale step
Crosstalk Rejection:	85 dB minimum, DC-1000Hz
Integral Nonlinearity:	±0.004 percent of FSR, maximum
Differential Nonlinearity:	±0.0015 percent of FSR, maximum

Analog Output Operating Modes and Controls

Clocking Modes:

Simultaneous Continuous Mode: Channel values in a designated channel group are stored in an intermediate buffer, and then are transferred to the output DAC's when an output clock occurs. The clock can be generated either by the internal rate generator, by a software flag, or by an external hardware trigger.

Simultaneous Burst Mode: A single function (i.e.: burst) is initiated by a software or hardware sync. During a burst, channel values in a designated channel group are stored in a transfer buffer, and then are transferred to the output DAC's each time a clock pulse is generated by the internal rate generator. The burst terminates when a Burst End flag is encountered

Channel-Sequential Modes: Same as simultaneous modes, except each value in the data buffer is written immediately to the associated output DAC. The group-end flag is ignored in this mode.

Channel Assignment:	A 3-bit field in the output buffer assigns the associated data field to a specific output channel.
Group End:	A single bit in the output buffer indicates the last value in a channel group.
Burst End:	A single bit in the output buffer indicates the last value in an output burst sequence.
Output Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported

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DIGITAL CONTROL OUTPUTS

Four digital output control lines provide TTL-level control of external devices, and support loading to 8mA.

PCI INTERFACE

Compatibility: Conforms to PCI Specification 2.3, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides single multifunction interrupt.
Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Power Requirements:

+5VDC ±0.2 VDC at 1.4 Amps, maximum, 0.9 Amps typical
Power Dissipation: 7.0 Watts maximum; 4.5 Watts typical

Mechanical Characteristics (PCI-104 or PC104-*Plus* form-factors):

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in)

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For example, model number PC104P-16AIO168-8-0-0-Nofilter-0 describes a PC104-*Plus* module with eight output channels, a 50-Pin IDC connector, no burst mode, no input filters, and a standard 30MHz master clock frequency.

Basic Model Number	Form Factor
PMC-16AIO168	PMC (Native)
PCI-16AIO168 [1]	PCI, short length
cPCI-16AIO168 [1]	cPCI, 3U
PCIe-16AIO168 [1]	PCI Express, short length
PCI104-16AIO168	PCI-104 (Native); No ISA passthrough
PC104P-16AIO168	PC104-*Plus* (Native)
PCIe104-16AIO168 [1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Analog Outputs [1]	No Output Channels	A = 0
	8 Output Channels	A = 8
System I/O Connector [1,2]	AMP 50-Pin IDC	B = 0
	68-Pin SCSI-3 [1]	B = SCSI3
Triggered Burst Mode [1]	No burst mode	C = 0
	Burst mode available	C = Burst
Input Filters [3]	Filters Installed	D = 0
	No input filters	D = Nofilter
Master Clock Frequency [4]	Standard: (30.000MHz)	E = 0 or 30.000M
	Custom: 29.988MHz	E = 29.988M

[1] May not appear in the product markings.
If all option fields are blank when ordered, the board will be supplied with eight analog output channels.

[2] PC104P is offered only with the 50-Pin IDC connector; PMC is offered only with the SCSI3 connector. Contact Sales for other options.

[3] Input filters are first order lowpass filters intended to reject cable noise. The cutoff frequency of approximately 180kHz is high enough to avoid interference in most applications. Without the input filters, the input bandwidth is on the order of 5MHz.

[4] ±50PPM.

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SYSTEM I/O CONNECTORS

50-Pin I/O Connector

(PC104P form factor)

Table 1. 50-Pin System I/O Connector

PIN	FUNCTION	PIN	FUNCTION
1	INPUT RTN	26	ANA OUT 02
2	INPUT RTN	27	ANA OUT 01
3	ANA INP 00 HI	28	ANA OUT 00
4	ANA INP 00 LO	29	OUTPUT RTN
5	ANA INP 02 HI	30	OUTPUT RTN
6	ANA INP 02 LO	31	VTEST
7	ANA INP 04 HI	32	DIFF TRIG IN LO
8	ANA INP 04 LO	33	VTEST RETURN
9	ANA INP 06 HI	34	DIFF TRIG IN HI
10	ANA INP 06 LO	35	INPUT RTN
11	ANA INP 08 HI	36	INPUT RTN
12	ANA INP 08 LO	37	INPUT RTN
13	ANA INP 10 HI	38	DIFF TRIG OUT HI
14	ANA INP 10 LO	39	TTL TRIG OUT
15	ANA INP 12 HI	40	DIFF TRIG OUT LO
16	ANA INP 12 LO	41	OUTPUT RTN
17	ANA INP 14 HI	42	DIG OUT 00
18	ANA INP 14 LO	43	TTL TRIG IN
19	INPUT RTN	44	DIG OUT 01
20	INPUT RTN	45	OUTPUT RTN
21	ANA OUT 07	46	DIG OUT 02
22	ANA OUT 06	47	OUTPUT RTN
23	ANA OUT 05	48	DIG OUT 03
24	ANA OUT 04	49	OUTPUT RTN
25	ANA OUT 03	50	DIGITAL RTN

Note: Analog inputs are shown for the differential input mode. In single-ended mode, LO inputs become consecutive odd-numbered channels, beginning with ANA INP 01 replacing ANA INP 00 LO.

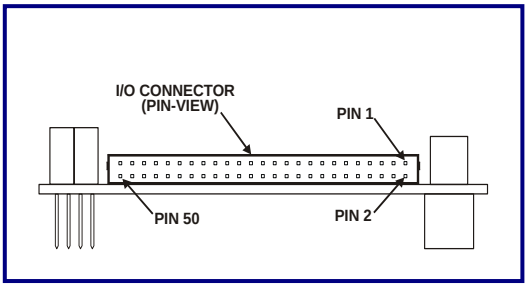

Figure 2. 50-Pin System I/O Connector

System Mating Connector:

Polarized 50-Pin socket connector:
AMP #1-746288-0,
with strain-relief #499252-4.

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SYSTEM I/O CONNECTORS (Continued)

68-Pin SCSI-3 I/O Connector

(PMC form factor)

Table 2. SCSI-3 System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INPUT RTN	1	DIGITAL RTN
2	INPUT RTN	2	DIG OUT 00
3	ANA INP 00 HI	3	DIGITAL RTN
4	ANA INP 00 LO	4	DIG OUT 01
5	ANA INP 02 HI	5	DIGITAL RTN
6	ANA INP 02 LO	6	DIG OUT 02
7	ANA INP 04 HI	7	DIGITAL RTN
8	ANA INP 04 LO	8	DIG OUT 03
9	ANA INP 06 HI	9	DIGITAL RTN
10	ANA INP 06 LO	10	TTL TRIG IN
11	INPUT RTN	11	DIGITAL RTN
12	INPUT RTN	12	TTL TRIG OUT
13	ANA INP 08 HI	13	DIGITAL RTN
14	ANA INP 08 LO	14	DIGITAL RTN
15	ANA INP 10 HI	15	DIFF TRIG IN LO
16	ANA INP 10 LO	16	DIFF TRIG IN HI
17	ANA INP 12 HI	17	DIGITAL RTN
18	ANA INP 12 LO	18	DIGITAL RTN
19	ANA INP 14 HI	19	DIFF TRIG OUT LO
20	ANA INP 14 LO	20	DIFF TRIG OUT HI
21	INPUT RTN	21	DIGITAL RTN
22	INPUT RTN	22	DIGITAL RTN
23	ANA OUT 07	23	SPARE 01 *
24	ANA OUT 06	24	SPARE 02 *
25	ANA OUT 05	25	SPARE 03 *
26	ANA OUT 04	26	SPARE 04 *
27	ANA OUT 03	27	SPARE 05 *
28	ANA OUT 02	28	SPARE 06 *
29	ANA OUT 01	29	SPARE 07 *
30	ANA OUT 00	30	SPARE 08 *
31	OUTPUT RTN	31	SPARE 09 *
32	OUTPUT RTN	32	SPARE 10 *
33	VTEST	33	SPARE 11 *
34	VTEST RETURN	34	SPARE 12 *

* Leave disconnected or connect to Digital Return.

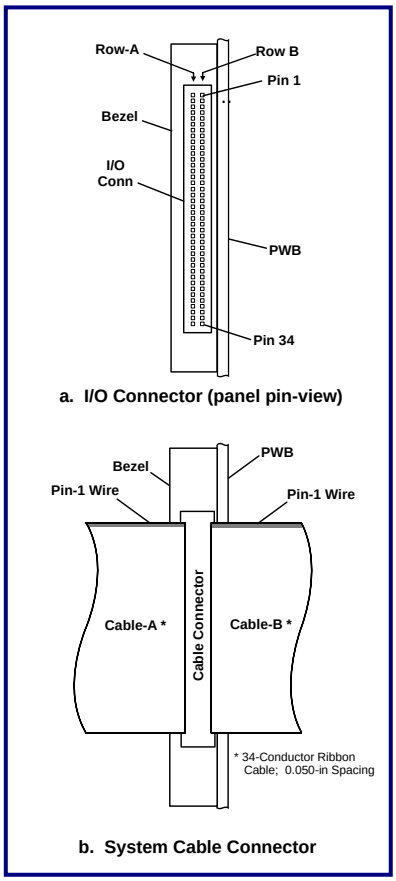

Figure 3. SCSI-3 System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7.

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