66-18AI64SSC750K

64-Channel, 18-Bit Simultaneous Sampling Analog Input Board

With 750 KSPS Sample Rate per Channel and 66 MHz PCI Support

Available also in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC66-18AI64SSC750K:	**PMC**, Single-width
PCI66-18AI64SSC750K:	**PCI**, short length
Cpci66-18AI64SSC750K:	**cPCI,** 3U
PC104P66-18AI64SSC750K:	**PC104-*Plus***
PCIe66-18AI64SSC750K:	**PCI Express**
PCIe10466-18AI64SSC750K:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details. Call for availability of other form factors, such as XMC, CCPMC, etc.

Features

- **64 Analog inputs with dedicated 18-Bit SAR ADC per Channel**
- **Simultaneous sampling of all inputs; Minimum Data Skew**
- **Sampling Rates to 750 KSPS per channel (48 MSPS aggregate rate)**
- **Continuous, Burst and Single-Sample Clocking Modes**
- **Software and I/O pinout compatibility with the 16AI64SSA/C**
- Selectable Differential Processing Simulates Differential Operation of Channel Pairs
- Input Ranges software-selectable as ±10V, ±5V, and 0 to +10V, or optionally as ±5V, ±2.5V , 0 to +10V, and 0 to +5V
- Hardware Sync I/O for Multiboard Operation
- FIFO buffer provides 256 K-Sample data capacity at 18 bits; 512K at 16 bits with data packing.
- A software-selectable low-latency configuration provides 64 registers that duplicate the last sample from all A/D converters
- 2-Channel DMA Engine
- Sampling and burst triggering controlled by internal rate generators, or by direct software control, or externally
- On-demand internal autocalibration of all channels
- Completely software-configurable; No field jumpers
- D32; 66MHz, 33MHz PCI compatibility, with universal 5V/3.3V Signaling
- Internal Sync/Clock I/O connector provides behind-panel access to clock and sync signals
- PMC version protected with integral EMI shield over analog components

Typical Applications

✓ High-Density Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Biometric Signal Analysis	✓ Dynamic Test Systems

- PRELIMINARY -

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General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Functional Description

The 18-Bit 66-18AI64SSC750K analog input board samples and digitizes 64 input channels simultaneously at rates up to 750,000 samples per second for each channel. Each input channel contains a dedicated 18-Bit sampling ADC, and the resulting 18-bit sampled data is available to the PCI bus through a 256 K-Sample FIFO buffer. Throughput capacity is further enhanced with 66MHz PCI support and increased local clocking frequency. All operational parameters are software configurable.

Inputs can be sampled in groups of 1, 2, 4, 8, 16, 32 or 64 channels; or software can select a first and last channel to be acquired. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±10V, ±5V, and 0 to +10V, or optionally as ±5V, ±2.5V, 0 to +10V, and 0 to +5V .

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections digitally during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

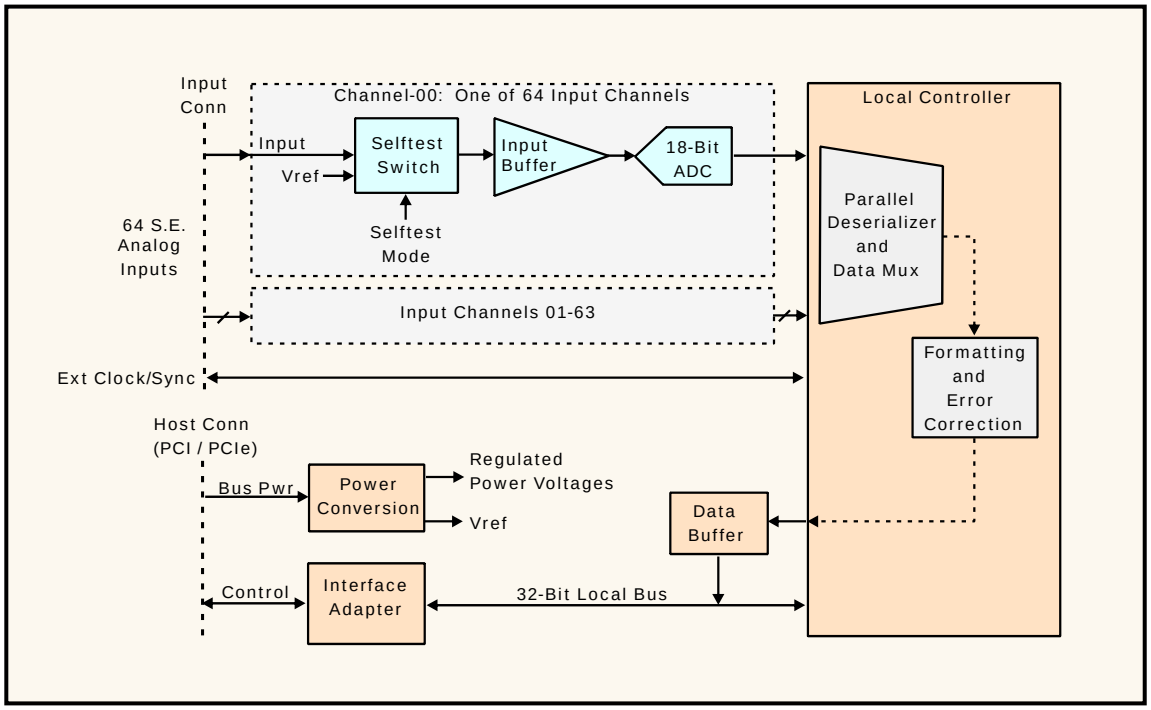

Figure 1. PM66-18AI64SSC750K; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3 for PMC, PC104 *Plus*, or PCI products, or with the PCIe Specification revision 2.0 for PCI Express products. System input/output connections are made at the front panel through a single high-density connector. Operation over the specified temperature range is achieved with conventional convection cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions, and with differential processing deselected

Input Characteristics:

Configuration:	64 single-ended analog input channels; Dedicated 18-Bit SAR ADC per channel. Optional 32-Channel version available.
Voltage Ranges:	Software configurable as ±10V, ±5V, 0 to +10V. (Optionally ±5V, ±2.5V, 0 to +10V, 0 to +5V
Input Impedance:	All input ranges: 350 KOhms minimum.
Bias Current:	(Inputs grounded; typical values): High Ranges: 8ua, 4ua, 0.3ua on ±10V, ±5V, 0 to +10V ranges, respectively. Low Ranges: 12ua, 7ua, 0.9ua, 0.5ua on ±5V, ±2.5V, 0 to +10V, 0 to +5V ranges.
Crosstalk Rejection:	90dB typical, DC-50kHz
Input Noise:	High range set (±10V) typical: 0.2 mVRMS; typical for bipolar ranges; 0.35mVRMS for unipolar ranges. 0.01-350kHz (91dB SNR on ±10V range). Low range set (±5V) typical: 0.15 mVRMS; typical for bipolar ranges; 0.25mVRMS for unipolar ranges. (Noise increases approximately 45-percent with differential processing selected).
Fault Protection:	Sustains ±40 Volts with power removed; ±25V with power applied.

Transfer Characteristics:

Resolution:	18 Bits (0.0004 percent of FSR)
Maximum Sample Rate:	750 KSPS per channel
Channels per Sample:	1, 2, 4, 8, 16, 32 or 64 channels, or first and last channel selection.

DC Accuracy: (Maximum composite error after autocalibration)

Range	Zero-Input *	Fullscale *
±10V	± 1.2mv	± 2.2mv
±5V	± 0.9mv	± 1.8mv
±2.5V	± 0.9mv	± 1.8mv
0/+10V	± 1.5mv	± 3.0mv
0/+5V	± 1.0mv	± 2.2mv

* Averaged values, referred to inputs. Typical values are approximately one-half the maximum values shown here.

Input Bandwidth (-3dB):	DC to 340 kHz typical. See ordering options for custom bandwidths.
Integral Nonlinearity:	±0.002 percent of FSR, maximum
Differential Nonlinearity:	±0.001 percent of FSR, maximum

Analog Input Operating Modes and Controls:

Input Data Buffers:	FIFO: 256 K-Samples in 18-Bit mode; 512 K-Samples in 16-Bit packed-data mode. An alternative 'Low-Latency' array of 64 data registers is available in addition to the FIFO.
Sample Clock Sources:	Internal rate generator; External Hardware Trigger I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generators:	Two 24-Bit Generators, Rate-A and Rate-B; both divide the master clock frequency to the required clock and trigger rates.
External TTL Sync:	Bidirectional TTL Sample Clock and Burst Trigger lines. These signals are duplicated internally through an internal Sync-I/O connector.
Internal Clock/Sync I/O:	Internal Sync-I/O connector provides internal (behind-panel) access to clock and sync signals.
Input Data Format:	Nonpacked Mode: 18-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed 16-BIt channel data. Even-numbered channels occupy the lower word (D00-15); odd channels occupy the upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.
Triggered Bursts:	Data can be acquired in triggered bursts, with up to 1,048,575 samples per burst, or in bursts of indefinite length.
Differential Processing:	A selectable processing option processes input data as 63 pseudo-differential channels (common return) or as 32 full-differential channels.

Host Control Interface Compatibility:

PCI, PMC, cPCI and PC104 *Plus*:

Conforms to PCI Specification 2.3, with D32 read/write transactions and universal 5V/3.3V signaling..
Supports block-mode DMA transfers as bus master. Provides a multifunction interrupt.

PCI Express:

PCIe Specification revision 2.0; single-lane.
Supports block-mode and demand-mode DMA transfers as bus master.

Physical Parameters

Power Requirements:

PCI, PMC, cPCI and PC104 *Plus form factors*:

+5.0 VDC ±0.25 VDC at: 1.1 Amps typical, 1.4 Amps, maximum

PCI Express Form Factor

+3.3±0.3VDC at 1.0 Amps typ; 1.2 Amps max. +12.0±0.8VDC at 0.2 Amp typ; 0.3 Amp max.

Physical Dimensions:

PMC Form Factor

Height: 13.5 mm (0.53 in),
Width: 74.0 mm (2.91 in)
Depth: 143.75 mm (5.66 in)

PCI Express Form Factor

Height: 12.4 mm (0.49 in)
Width: 110.1 mm (4.37 in)
Depth: 167.6 mm (6.60 in)

Environmental Specifications:

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D-E", as indicated below. For example, model number PMC66-18AI64SSC750K-64-60.00M-340K-RTN-5V describes a board with 64 input channels, a standard 60MHz master clock frequency, standard 340kHz bandwidth, Standard INP RTN pin, ±5V maximum input range, and no custom features.

Basic Model Number	Form Factor
PMC66-18AI64SSC750K	PMC (Native)
PCI66-18AI64SSC750K [1]	PCI, short length
Cpci66-18AI64SSC750K [1]	cPCI, 3U
PCIe66-18AI64SSC750K [1]	cPCI, 3U
PC104P66-18AI64SSC750K	PC104-*Plus*
PCIe10466-18AI64SSC750K [1, 2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	64 Channels	A = 64
	32 Channels	A = 32
Master Clock Frequency [1]	60.00 MHz	B = 60M
	---	B = (XX.XXX MHz)M
Custom Input Bandwidth, -3dB [2]	Standard 340kHz	C =340K
	70kHz	C = 70K
	---	C = (Freq, kHz)K
INPUT RTN / CLK I/O Pin B33 configuration	Configured as an INPUT RTN pin	D = RTN
	Configured as an active CLK I/O pin.	D = CLK
Input Ranges	Selectable as: ±10V, ±5V, 0 to +10V	E = 10V or 0 (Zero)
	Selectable as: ±5V, ±2.5V, 0 to +10V, 0 to +5V	E = 5V
Custom Feature	No custom features	F = 0 (Zero) or blank

[1] Custom clock frequencies available from 58-62MHz. Call for availability.

[2] Custom bandwidths available from 10kHz to 1.0MHz. ±20%. Call for availability.

Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	INP00
2	INP01
3	INP02
4	INP03
5	INPUT RTN
6	INP04
7	INP05
8	INP06
9	INP07
10	INPUT RTN
11	INP08
12	INP09
13	INP10
14	INP11
15	INPUT RTN
16	INP12
17	INP13
18	INP14
19	INP15
20	INPUT RTN
21	INP16
22	INP17
23	INP18
24	INP19
25	INPUT RTN
26	INP20
27	INP21
28	INP22
29	INP23
30	INPUT RTN
31	INP24
32	INP25
33	INP26
34	INP27
35	INPUT RTN
36	INP28
37	INP29
38	INP30
39	INP31
40	INPUT RTN

ROW-B	
PIN	SIGNAL
1	INP32
2	INP33
3	INP34
4	INP35
5	INPUT RTN
6	INP36
7	INP37
8	INP38
9	INP39
10	INPUT RTN
11	INP40
12	INP41
13	INP42
14	INP43
15	INPUT RTN
16	INP44
17	INP45
18	INP46
19	INP47
20	INP48
21	INPUT RTN
22	INP49
23	INP50
24	INP51
25	INP52
26	INP53
27	INPUT RTN
28	INP54
29	INP55
30	INP56
31	INP57
32	INP58
33	INPUT RTN / CLK I/O [1]
34	INP59
35	INP60
36	INP61
37	INP62
38	INP63 / CLK I/O [2]
39	TRIG I/O RTN
40	TRIG I/O

[1] This pin can be factory configured either as an INPUT RTN. pin or as a CLK I/O pin. See ordering options. (Note: Configuring this pin as a CLK I/O pin prevents 100% pin-compatibility with the 16AI64SSC board).

[2] Software-programmable as either analog Input Channel 63, or as a TTL bidirectional CLK I/O pin.

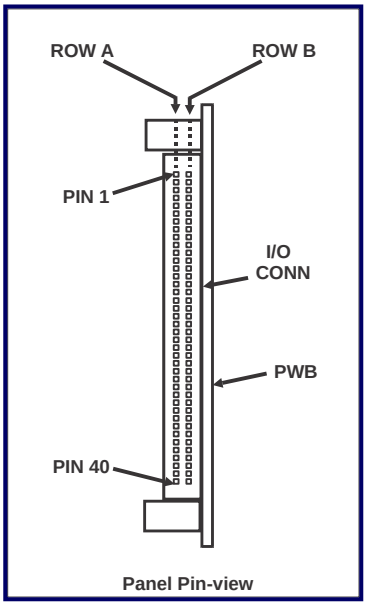

Figure 2. System Input Connector

System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket connector:
3M# P50E-080S-EA,
or equivalent.

Table 2. Internal Sync-I/O Connector

SYNC-I/O CONN PIN [1]	SIGNAL
1	DIG RTN
2	AUX CLOCK
3	DIG RTN
4	AUX TRIGGER
5	DIG RTN
6	Reserved. Connect to INPUT RTN or leave disconnected.

8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com