

## ***cPCI6U64-24DSI20C500K***

### **24-Bit, 20-Channel, 500KSPS, cPCI 6U Analog Input Module**

*With 20 Delta-Sigma Input Channels*

#### ***Features Include:***

- 20 Multirange differential 24-Bit simultaneously-sampled analog input channels.
- Input sample rates from 10 to 500 Kilosamples per second per channel, software-selectable; including 327.680 KSPS.
- Fixed  $\pm 6V$  input range. Contact factory for availability of optional input range of  $\pm 10V$ ,  $\pm 5V$  or  $\pm 2.5V$ .
- Delta-Sigma input conversion minimizes or eliminates the need for antialias filtering.
- 512K-sample analog input FIFO buffer.
- Continuous and Burst (One-shot) sampling modes.
- Sample clock source selected as internal or external.
- Supports multiboard synchronization of analog inputs.
- On-demand internal offset and gain autocalibration of all analog inputs.
- Software-controlled Front-Panel LED indicator.
- 8-Bit bi-directional digital TTL port.
- cPCI 6U form factor. (**Contact factory for availability in PCI and PCI-Express form factors**).
- Front-Panel system I/O connections,
- 66MHz 64-bit PCI support, with universal 5V/3.3V signaling and DMA support. PCI burst rates to 400MB/sec.

#### ***Applications:***

- |                 |                       |                           |
|-----------------|-----------------------|---------------------------|
| ✓ Sonar Arrays  | ✓ Voltage Acquisition | ✓ Phase Comparison        |
| ✓ Analog Inputs | ✓ Acoustic Research   | ✓ Audio Waveform Analysis |

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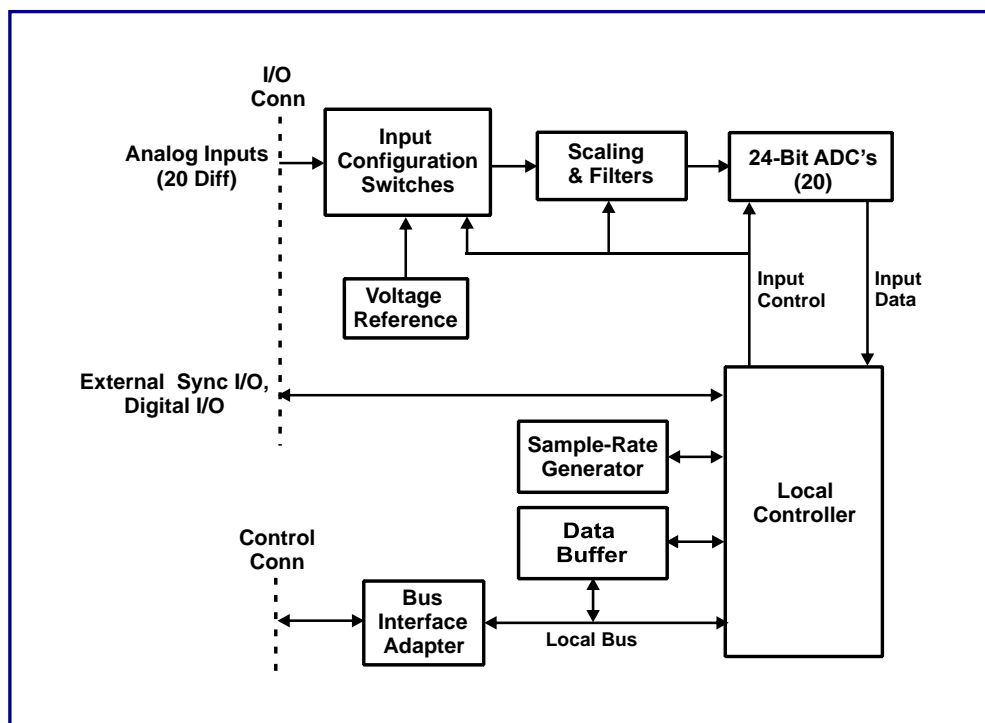
## Overview:

The 20-channel cPCI6U64-24DSI20C500K analog input module provides high-density 24-bit analog input resources on an industry-standard module. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms.

## Functional Description:

Each of 20 analog input channels contains a lowpass analog image filter and a delta-sigma A/D converter that provides inherent antialias suppression and sharp cutoff lowpass filtering. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter rejects those interference signals that fall within the harmonic images of the digital filter.

An internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 10KSPS to 500KSPS. Conversion data from all active channels is transferred to the PCI bus through a 512K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command or by external hardware sync and clock input signals.



**Figure 1. cPCI6U64-24DSI20C500K; Functional Organization**

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

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## ***ELECTRICAL SPECIFICATIONS***

At +25 °C, with specified operating conditions.

### ***Input Characteristics:***

Configuration:	20 two-wire differential input channels. 12, 8 and 4-channel configurations also available.
Voltage Range:	Fixed $\pm 6V$ input range. Contact factory for availability of optional input range of $\pm 10V$ , $\pm 5V$ or $\pm 2.5V$ .
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	62dB to 15kHz on $\pm 6V$ range; typical
Common Mode Range:	$\pm 10$ Volts with zero normal-mode input
Overvoltage Protection:	$\pm 35$ -Volt transients with power applied; $\pm 30$ Volts with power removed

### ***Transfer Characteristics:***

Conversion Architecture:	24-Bit Delta-Sigma		
Sample Rate:	10-500 kilosamples per second per channel, software-selectable, including 327.680KSPS		
Oversampling Factor:	x256 (10-78KSPS), x128 (78-156KSPS), x64 (156-312KSPS), x32 (312-500KSPS),		
DC Accuracy: (Mean composite error after autocalibration)	Input Range	Midrange (Zero) Accuracy	$\pm$ Fullscale Accuracy
	$\pm 6V$	$\pm 1.2mv$	$\pm 4.0mv$
Passband:	DC to 40% of the sample rate at -0.1dB, or 41% at -3dB; Typical.		
Passband Ripple:	$\pm 0.05dB$ maximum		
Stopband threshold:	Typically 50 percent of the selected sample rate.		
Stopband Attenuation:	110dB Typical		
Integral Nonlinearity (INL)	0.001 percent of fullscale range; typical.		
No Missing Codes	24 Bits.		
Dynamic Range:	Typical with DC-50kHz bandwidth: 107dB with oversampling at x256; 102dB at x32. $\pm 6V$ range; typical with DC-50kHz bandwidth		
SINAD:	102dB with oversampling at x256; 99dB at x32. $\pm 6V$ range; Typical with DC-50kHz bandwidth		
Interchannel Crosstalk:	-96dB typical to 40kHz		
Phase Skew:	Typically less than 100ns (0.1-Degree for $F_{sig} = 5kHz$ ), with $F_{sig}/F_{samp} < 0.35$ ; channel-channel (board-board for multiboard configurations), excluding noise.		
Antialias Filtering:	Each ADC provides linear-phase digital lowpass filtering as indicated for "passband" and "stopband". In addition to the digital filter, a single-pole lowpass analog image filter in each channel provides a -3dB cutoff frequency of approximately 2MHz to suppress images from the digital filter. Optional alternative filter frequencies are available, and should be selected to be well above the expected passband.		
Input Data Buffer:	512 K-Sample FIFO buffer.		

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## ***Operating Modes and Controls:***

Organization:	All input channels operate at the same sample rate, controlled by division of an internal or external rate generator frequency.
Sampling Clock I/O:	The sampling clock can be derived either from an internal rate generator, or from a TTL or LVDS external hardware input. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.
Internal Rate Generator:	An internal PLL rate generator provides sample rates from 2 KSPS to 500 KSPS. The frequency of the generator is controlled by an internal reference oscillator, the ratio of two 10-Bit integers, and an integer divisor, with a setting accuracy of 25 PPM.
Synchronization:	Daisy-chained or 'star-configuration' hardware sync inputs and outputs can be used to synchronize sampling among multiple boards.
Burst Timing:	Triggered burst sampling can be timed either internally or externally.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A 5-bit channel tag is appended to each input data value.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.
LED Indicator:	Software-controlled front-panel red LED indicator. Defaults to ON.
Digital I/O	Eight TTL I/O lines in two groups of four bits, group-configurable as inputs or outputs. 0.2ma maximum input loading as current source, 8ma output loading as either source or sink. Direct register control.

## ***Bus Compatibility:***

Conforms to PCI Specification 2.3: D32/64, 33/66MHz, 64-bit /32-Bit, universal (3.3V/5V) signaling.  
Conforms to PICMG Specification Version 2.0, Revision 3.0.  
Provides Two-Channel DMA as bus master in block and demand modes.  
Geographic addressing and Hot-Swap functions are not supported.

*(Contact factory for availability in PCI and PCI-Express form factors).*

## ***Power Requirements:***

+5.0 VDC  $\pm$ 0.25 VDC at:

20-Channel Configuration: 4.4 Amps typical, 5.2 Amps, maximum

4-Channel Configuration: 1.7 Amps typical, 2.0 Amps, maximum

## ***Physical Dimensions (cPCI 6U):***

Height: 233.3 mm  
Depth: 21.6 mm  
Width: 160.0 mm .

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## Environmental Specifications:

Ambient Temperature Range:

Standard Temperature:

Operating: 0 to +70 Degrees Celsius \*

Storage: -40 to +85 Degrees Celsius

Extended Temperature:

Operating: -40 to +80 Degrees Celsius \*

Storage: -40 to +85 Degrees Celsius

\* Air temperature at board surface.

Relative Humidity:

0 to 95%, non-condensing

Altitude:

Operation to 10,000 ft.

Cooling:

Conventional air cooling; 150 LFPM

## Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number cPCI64-24DSI20C500K-20-SF-6V-0 describes a 6U cPCI module with 20 input channels, standard image filter frequency, a fixed  $\pm 6V$  input range, and no custom features. For industrial (extended) temperature operation, add "-I" at the end of the model number.

**Table 1. Ordering Options**

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Channels	A = 4
	8 Channels	A = 8
	12 Channels	A = 12
	20 Channels	A = 20
Image Filter -3dB Frequency	Standard 2.0MHz (-0.1dB at 300kHz)	B = SF
	Custom Frequencies:	B = CF <sub>x</sub> <sup>1</sup>
Input Range Set	Fixed $\pm 6V$ input range	C = 6V
	(Custom fixed input range)	C = (TBD)
Custom Features <sup>2</sup>	---	D = 0

<sup>1</sup> "x" = Filter frequency.  $\pm 15\%$  frequency accuracy. Contact factory for availability of specific frequencies.

<sup>2</sup> Contact factory for availability.

Note: The range of sample rates is software-selectable from 10-500KSPS, including an exact value of 327.680KSPS (within the reference oscillator frequency tolerance of  $\pm 25\text{PPM}$ ).

# SYSTEM INTERFACE CONNECTORS

**Table 2. System I/O Connectors**

FP-P1		FP-P2	
Pin	Signal	Pin	Signal
1	INP CH 00 HI	1	INP CH 10 HI
34	INP CH 00 LO	34	INP CH 10 LO
18	INP RETURN	18	INP RETURN
2	INP RETURN	2	INP RETURN
35	INP CH 01 HI	35	INP CH 11 HI
19	INP CH 01 LO	19	INP CH 11 LO
3	INP RETURN	3	INP RETURN
36	INP RETURN	36	INP RETURN
20	INP CH 02 HI	20	INP CH 12 HI
4	INP CH 02 LO	4	INP CH 12 LO
37	INP RETURN	37	INP RETURN
21	INP RETURN	21	INP RETURN
5	INP CH 03 HI	5	INP CH 13 HI
38	INP CH 03 LO	38	INP CH 13 LO
22	INP RETURN	22	INP RETURN
6	INP RETURN	6	INP RETURN
39	INP CH 04 HI	39	INP CH 14 HI
23	INP CH 04 LO	23	INP CH 14 LO
7	INP RETURN	7	INP RETURN
40	INP RETURN	40	INP RETURN
24	INP CH 05 HI	24	INP CH 15 HI
8	INP CH 05 LO	8	INP CH 15 LO
41	INP RETURN	41	INP RETURN
25	INP RETURN	25	INP RETURN
9	INP CH 06 HI	9	INP CH 16 HI
42	INP CH 06 LO	42	INP CH 16 LO
26	INP RETURN	26	INP RETURN
10	INP RETURN	10	INP RETURN
43	INP CH 07 HI	43	INP CH 17 HI
27	INP CH 07 LO	27	INP CH 17 LO
11	INP RETURN	11	INP RETURN
44	INP RETURN	44	INP RETURN
28	INP CH 08 HI	28	INP CH 18 HI
12	INP CH 08 LO	12	INP CH 18 LO
45	INP RETURN	45	INP RETURN
29	INP RETURN	29	INP RETURN
13	INP CH 09 HI	13	INP CH 19 HI
46	INP CH 09 LO	46	INP CH 19 LO
30	INP RETURN	30	INP RETURN
14	INP RETURN	14	INP RETURN
47	DIGITAL GND	47	DIGITAL GND
31	DIGITAL GND	31	DIGITAL GND
15	DIO 00	15	DIO 04
48	DIGITAL GND	48	DIGITAL GND
32	DIO 01	32	DIO 05
16	DIGITAL GND	16	DIGITAL GND
49	DIO 02	49	DIO 06
33	DIGITAL GND	33	DIGITAL GND
17	DIO 03	17	DIO 07
50	DIGITAL GND	50	DIGITAL GND

<sup>1</sup> In single-ended mode, 'HI' indicates signal, and 'LO' indicates no-connect.

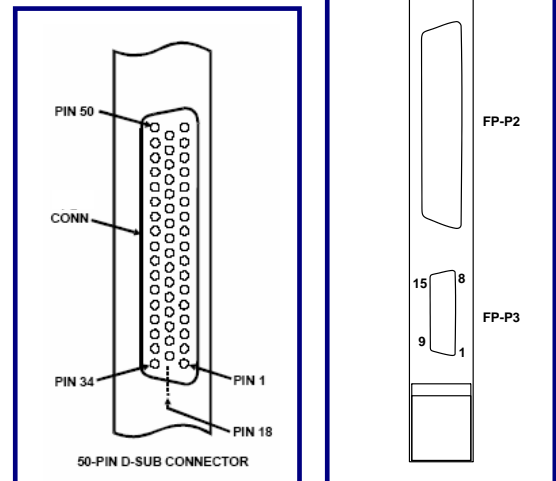
**System Cable Mating Connectors:**

50-Pin D-Subminiature IDC connector:  
Tyco # 1658607-1,  
with strain-relief: Tyco # 746785-1.

15-Pin D-Subminiature IDC connector:  
Tyco # 1658608-3,  
with strain-relief: Tyco # 747275-3.

**Table 3. Sync I/O Connector FP-P3  
(15-Pin D-Sub)**

Pin	Signal
1	EXT SYNC INPUT HI
9	EXT SYNC INPUT LO
2	DIGITAL GND
10	DIGITAL GND
3	EXT CLK INPUT HI
11	EXT CLK INPUT LO
4	DIGITAL GND
12	DIGITAL GND
5	EXT SYNC OUT HI
13	EXT SYNC OUT LO
6	DIGITAL GND
14	DIGITAL GND
7	EXT CLK OUT HI
15	EXT CLK OUT LO
8	DIGITAL GND



**Figure 2. I/O Connectors**

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