



## AV 107

Phased-Array Radar-Receiver  
EW-ESM

3U VPX  
Virtex 7 FPGA  
Quad 12 bit 2.5 Gsps ADC  
Conduction or Air-Cooled

#### Applications

- Real time processing
- Electronic Warfare
- Radar receiver
- LIDAR
- Instrumentation

#### Features

- 4 channels 2.5 Gsps 12-bit ADC
- 4 independent Digital Down Converters, 120 or 240 MHz BW
- 4 independent Low jitter clock synthesizers
- 4 External clock input/output
- External and internal reference
- External trigger input with TDC
- User programmable Xilinx® Virtex® 7 VX415T or VX690T FPGA
- 667 MHz 256M32 DDR3 SDRAM
- 3U OpenVPX standard compliant
- Air cooled and Conduction cooled rugged versions

#### 12-bit 2.5 Gsps Analog-Digital Converters

The AV107 Analog to Digital conversion is performed by four 12-bit 2.5 Gsps ADCs with independent 120 or 240 MHz Bandwidth Digital Down Converters.

The AV107 provides four front panel SMPM connectors for analog inputs.

Single ended input signals are AC coupled with an input bandwidth from 1 MHz to more than 5.5 GHz with 9 dBm input level.

A wideband signal generator is provided for on board, stand-alone calibration.

#### Clock

The AV107 provides four independent ultra-low jitter clock synthesizers locked on a 100 MHz internal reference.

The AV107 provides a front panel SMPM connector for external reference, 10 to 100 MHz as well as a VPX P2 reference input.

Four SMPM connectors support either external clock inputs for the ADCs or clock output when the internal clock synthesizers are used. External clock from 1 GHz to 2.5 GHz are supported.

Dedicated fine clock phase controls on each channel allow for accurate adjustment of phase delay between all channels.

#### Trigger and Synchronization

The AV107 supports a differential pair on VPX P2 connector used as a trigger signal. An embedded Time to Digital Converter with a 15 ps resolution allows for fine synchronisation on external event.

#### FPGA

The AV107 is fitted with a Xilinx Virtex 7 VX415T or VX690T user programmable FPGA. Only few resources are used to control and communicate with external hardware

#### Overview

The AV107 is part of ApisSys' range of High Speed data conversion and signal processing solutions based on the VITA 46, VPX standard.

The AV107 is fully compliant with OpenVPX standard, accommodating various communication protocols such as PCIe, SRIO, 1 Gbit and XAU1 10 Gbit Ethernet, as well as non OpenVPX adopted standard such as Aurora.

The AV107 combines four 12-bit 2.5 Gsps ADCs with ultra high processing power delivered by Xilinx® Virtex® 7 FPGA, making it ideally suited for fully synchronous multiple channels test and measurement, Electronic Warfare, Ultra Wideband Radar Receivers or LIDAR applications.

The AV107 features an internal ultra low jitter reference and four independent clock synthesizers and can be used with either external clocks or external reference for higher flexibility.

The AV107 supports an external trigger signal coupled with a 15ps resolution Time to Digital Converter (TDC).

The AV107 includes one Xilinx® Virtex® 7 FPGA VX415T or VX690T for an impressive processing capability of more than 2 TMACs (Multiply Accumulate per second), one high speed 256M32 DDR3 SDRAM memory for data processing and a 1 Gb synchronous FLASH memory for multiple firmware storage.

The AV107 provides a USB 2.0 interface and a 10/100 Ethernet interface intended to be used for system monitoring and supervision.

The AV107 comes with complete software drivers for Windows and Linux. An FPGA Development Kit is provided including all necessary cores to build user FPGA application.

such as DDR3 SDRAM and monitoring subsystem, leaving most of the logic and block RAM and all DSP resources available for customer processing.

Dedicated to signal processing, the Xilinx Virtex 7 VX415T FPGA includes 412,160 logics cells, 880 bloc RAM (36 Kbit each), 2,160 DSP48E1 slices and 2 PCIe interface blocs.

The most powerful version embeds a Xilinx Virtex 7 VX690T which provides 693,120 logics cells, 1,470 bloc RAM and 3,600 DSP48E1 slices for an impressive processing power of more than 2 TMACs.

The FPGA is delivered in -2 speed grade.

#### Memories

The AV107 includes one 667 MHz 256M32 DDR3 SDRAM memory banks and one 1 Gbit synchronous BPI FLASH used to store multiple FPGA configuration files.

#### VPX interface

The AV107 features an OpenVPX VITA 65 compliant interface with support for two Fat Pipes for Data Plane, one Fat Pipe for Expansion Plane, two Ultra Thin Pipes for Control Plane and two User Defined Ultra Thin Pipes on P1. The AV107 also supports a USB2.0, a 10/100 Ethernet and 24 LVDS differential pairs on P2.

The AV107 features two low phase noise clock generators able to synthesize clock references for the FPGA GTXs from 100 MHz to 312.5 MHz, allowing support of all major protocols such as Aurora, GigE, PCIe Gen 1 and Gen 2, SATA, SRIO and XAU1 10Gbit Ethernet up to 12.5 Gbps.

#### Microcontroller

The AV107 features a 32-bit 80 MHz microcontroller used primarily for board monitoring

and supervision.

The microcontroller supports a USB 2.0 and a 10/100 Ethernet interfaces accessible on the VPX P2 user IO pins through an ApisSys AR102 Rear Transition Module or an ANSI/VITA 46.10 compliant custom RTM board.

The microcontroller firmware includes all necessary features for board monitoring and supervision.

#### Firmware

The AV107 comes with a firmware package which includes VHDL cores allowing for control and communication with all AV107 hardware resources.

A base design is provided which demonstrates the use of the AV107 and gives users a starting point for firmware development. The AV107 firmware package is supported on the Xilinx VIVADO® 2013.4 design suite and later.

#### Software

The AV107 is delivered with software drivers for Windows 7 and Linux.

#### Ruggedization

The AV107 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6, ECC3 and ECC4.



## Specifications

### Analog Inputs

- Input coupling: AC
- Full power bandwidth > 5.5 GHz
- Full scale : 9 dBm
- Impedance: 50 Ohm
- Connectors: SMPM

### Analog-Digital Conversion

- Quad channels,  $F_s \leq 2.5$  GHz
- Resolution: 12 bit
- Sampling Performances @1 GHz
  - SNR: 58.5 dBFS
  - SFDR: 69 dBc
  - ENOB: 9.3 bits

### Clock

- Internal:
  - Four independent synthesizers,
  - 1 GHz to 2.5 GHz low jitter clock
- External Input/Output Clocks:
  - frequency: 1 GHz to 2.5 GHz
  - Input clock : 10 dBm recommended
  - Connector: SMPM, 50 Ohm
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Connector: SMPM, 50 Ohm and VPX P2.

### Digital Down Converter

- 4 independent DDC:
  - Tuning frequency step:  $F_s/1024$
  - 120 or 240 MHz Bandwidth DDC with  $F_s/8$  decimation at 2.5 Gsps

### Trigger

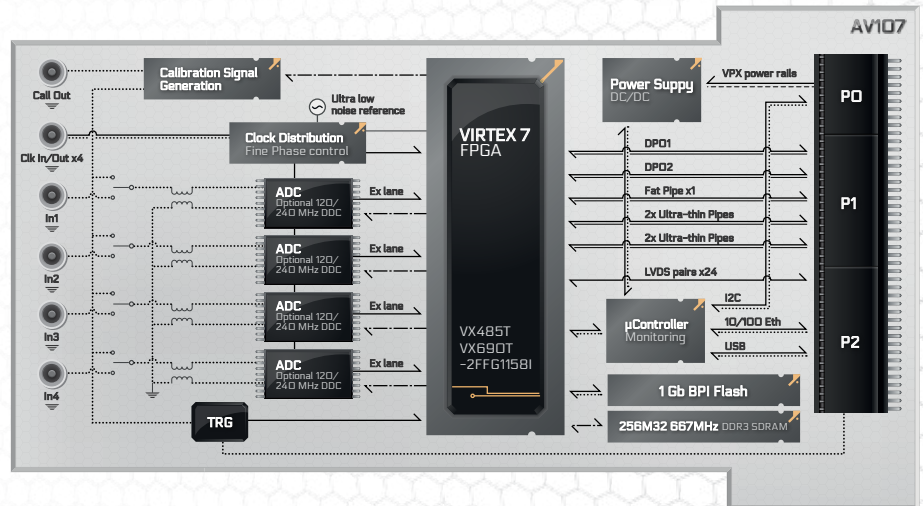
- External: 0 to 2Vp
- Connector: SMPM, 50 Ohm

### FPGA

- FPGA: Xilinx Virtex 7
  - XC7VX415T-2FFG1158 or
  - XC7VX690T-2FFG1158

### Memory

- 1 bank 256M32 DDR3 SDRAM, 667 MHz clock
- One 1 Gbit NOR FLASH memory



### VPX interface

- P1:
  - Data plane: two fat pipes
  - Expansion plane: one fat pipe
  - Control plane: 2 ultra-thin pipes
  - 2 user-defined ultra-thin pipes
- P2:
  - USB2.0 and 10/100 Ethernet
  - 24 LVDS differential pairs

### Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

### Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2013.4 and later

### Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3 and ECC4

### Power dissipation

- +12V: 6.1 A max (72.8W)
- +5V: 8.7 A max (43.7W)
- +3.3V: 0.5 A max (1.8W)
- +3.3VAUX: 0.3 A max (1.1W)

### Weight

- Air cooled : 550g
- Conduction cooled : 650g

## Ordering information

| Part Number         |                        | A | V | 107 | - | rr | - | a |
|---------------------|------------------------|---|---|-----|---|----|---|---|
| Ruggedization level | Air Standard           | - | - | -   | - | AS | - | - |
|                     | Air Rugged             | - | - | -   | - | AR | - | - |
|                     | Conduction Standard    | - | - | -   | - | CS | - | - |
|                     | Conduction Rugged      | - | - | -   | - | CR | - | - |
| Options 1           | FPGA Virtex 7 VX415T-2 | - | - | -   | - | -  | - | 1 |
|                     | FPGA Virtex 7 VX690T-2 | - | - | -   | - | -  | - | 2 |



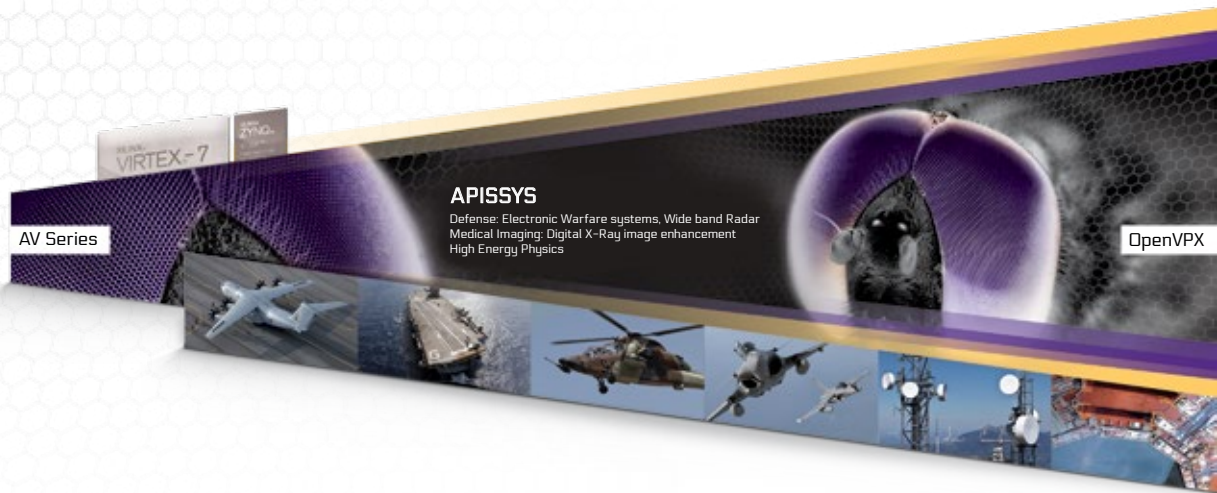
# High Speed Data Conversion & Signal Processing Solutions

## Ruggedization levels

|                                 | Air flow, Standard<br>AS (VITA 47 EAC4)   | Air flow, Rugged<br>AR (VITA 47 EAC6)   | Conduction Standard<br>CS (VITA 47 ECC3)   | Conduction Rugged<br>CR (VITA47 ECC4)  |
|---------------------------------|---|---|--|--|
| Operating Temperature           | 0°C to +55°C (1)<br>(10 CFM airflow at sea level)                               | -40 to +70°C (1)<br>(20 CFM airflow at sea level)                                 | -40°C to +70°C<br>(Card Edge)  | -40°C to +85°C<br>(Card Edge)  |
| Non Operating Temperature       | -40°C to +85°C  | -50°C to +100°C   | -50°C to +100°C  | -55°C to +105°C  |
| Operating Vibration<br>(Random) | 5Hz - 100Hz +3 dB/octave<br>100Hz-1kHz = 0.04 g2/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.04 g2/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.1 g2/Hz<br>1kHz - 2kHz -6 dB/octave | 5Hz - 100Hz +3 dB/octave<br>100Hz - 1kHz = 0.1 g2/Hz<br>1kHz - 2kHz -6 dB/octave |
| Operating Shock                 | 20g, 11 millisecond, half-sine  | 20g, 11 millisecond, half-sine  | 40g, 11 millisecond, half-sine   | 40g, 11 millisecond, half-sine   |
| Operating Relative Humidity     | 0% to 95%<br>non-condensing   | 0% to 95%<br>non-condensing   | 0% to 95%<br>non-condensing  | 0% to 95%<br>non-condensing  |
| Operating Altitude              | @ 0 to 10,000 ft<br>with adequate airflow                                       | @ 0 to 30,000 ft<br>with adequate airflow   | @ 0 to 30,000 ft   | @ 0 to 60,000 ft   |
| Conformal Coating               | No  | Optional (default acrylic AVR80)  | Yes (default acrylic AVR80)  | Yes (default acrylic AVR80)  |

[www.apissys.com](http://www.apissys.com)

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