Model 5560

3U VPX SOSA aligned processor board with Versal HBM ACAP

Co-processor for distributed ACAP processing tasks

- High-Bandwidth Memory (HBM) delivers 8x more memory bandwidth than traditional DDR5 solutions
- Board interfaces: 1 GigE, 10 GigE, 40 GigE, 100 GigE, and PCIe
- High-bandwidth memory, ACAP logic, and DSP density provide robust processing in a single slot
- Expansion mezzanine interface for data converter or digital I/O boards

The 5560 is a high-performance, SOSA aligned 3U OpenVPX co-processor board based on the Xilinx Versal HBM ACAP (Adaptive Compute Acceleration Platform). It serves as an ideal stand-alone processor or as a co-processor for distributed ACAP processing tasks.

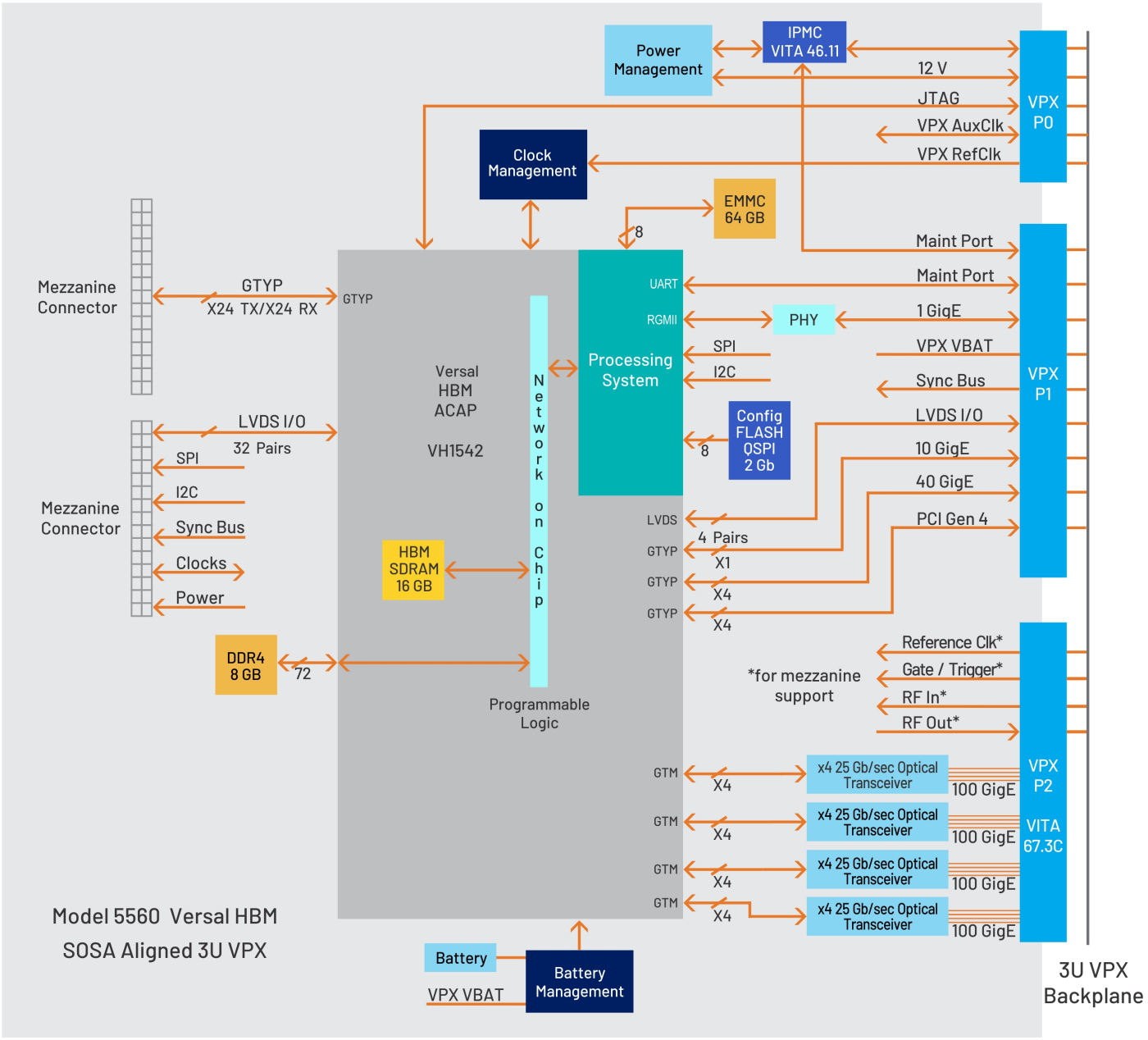
Ample data transfer bandwidth and flexibility are provided by a range of board interfaces including 1 GigE, 10 GigE, 40 GigE, 100 GigE, and PCIe with installation of Mercury or user-supplied IP. The Versal HBM's on-chip high-bandwidth memory coupled with the ACAP's logic and DSP density enable the 5560 to provide robust processing in a single 3U VPX slot.

FEATURES

- Features Xilinx Versal HBM ACAP
- 10 GigE Interface and 40 GigE Interface
- Optional VITA 67.3C optical interface for backplane gigabit serial communication
- Up to 4 100 GigE UDP Interfaces
- Compatible with several VITA standards including: VITA 46.11, VITA 48, VITA 67.3C and VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled
- Navigator Design Suite for software and custom IP development
- Expansion mezzanine interface for data converter or digital I/O boards

SOSA™ Sensor Open Systems Architecture

5560 BLOCK DIAGRAM



BOARD ARCHITECTURE

The 5560 board design places the Versal HBM ACAP as the cornerstone of the architecture. All control and data paths are accessible by the ACAP. IP and software are provided to access all board interfaces including PCIe, 10 and 40 GigE. Optional 4-lane optical interfaces are also available and each provides a 100 GigE UDP interface with an IP core included with the Navigator FPGA Design Kit.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kits (FDKs) include the board's FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Mercury factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5560's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

XILINX VERSAL HBM ACAP

The 5560 features the Versal HBM ACAP. The ACAP provides 16 GB of on-chip HBM SDRAM and supports memory bandwidth of up to 820 GB/s. This represents better than an 8X throughput increase over traditional, external DDR5 SDRAM. This increased performance addresses the ever-accelerating memory requirements of high bandwidth, high computation applications. Additional resources include 7392 DSP slices, 3.8 million system logic cells and 32.7 Gb/s GTYP gigabit serial transceivers.

INTEGRATED PLATFORM MANAGEMENT CONTROLLER

The 5560 uses an Integrated Platform Management Controller (IPMC) to provide a fully compliant and flexible management solution for Field Replaceable Units (FRU) that support the VITA 46.11 standard required by HOST and SOSA architectures. The IPMC provides a standardized implementation of FRU management interfaces, control signals and sensor monitoring.

The IPMC provides the Chassis Manager and higher-level System Management Software (SMS) access to FRU information, FRU control signals and sensor monitoring functions so that they can identify, activate/de-activate, reset and monitor the health of the card and take appropriate system control actions.

The IPMC also provides a low-level path for configuration management and FRU maintenance through both IPMI messages and a Maintenance Port (MP) serial interface. The maintenance port provides a terminal mode command-line interface and supports monitoring, data uploads and FRU-level troubleshooting.

EXPANSION MEZZANINE

The 5560 features an expansion mezzanine to host analog data converters or additional optical or digital interfaces. The mezzanine connectors provide 24 gigabit serial lanes at 32 Gb/sec ideal for supporting high bandwidth A/Ds and D/As. Additional signals including 32 LVDS pairs and clock and sync signals provide flexibility to support a range of different converters and architectures.

SPECIFICATIONS

Adaptive Compute Acceleration Platform (ACAP)

Type: Xilinx/AMD Versal HBM VH1542

Adaptable Engines: 3,837 k System Logic Cells

Intelligent Engines: 7,392 DSP slices

Scalar Engines:

- Dual-core ARM Cortex-A72
- Dual-core ARM Cortex-R5F

HBM DRAM: 16 GBytes

Total Block RAM: 89 Mb

UltraRAM: 366 Mb

ACAP I/O

Interface: GPIO

- Quantity: 4 pairs
- Type: LVDS
- Location: VPX-P1

Interface: 1 GigE

- Location: VPX-P1

Interface: 10 GigE

- Location: VPX-P1

Interface: 40 GigE

- Location: VPX-P1

Interface: PCI-Express

- Type: Gen 1, 2, 3, or 4: x4
- Location: VPX-P1

Interface: Optical

- Quantity: 16 full duplex lanes
- Speed: 25 Gb/sec
- Laser: 850 nm
- Location: VITA 67.3C (VPX-P2)

Memory

ECCM: 64 GBytes

SDRAM: DDR4, 8 GBytes

Configuration FLASH: 2x 1 Gbit QSPI

Environmental

Option -763:L3a (conduction-cooled)

- Operating Temp: 0° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions: VPX board

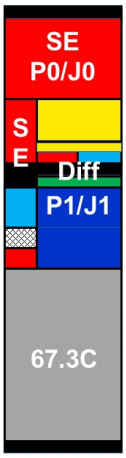
- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)

Weight: TBD

OpenVPX Compatibility

The 5560 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-1F1U1S1S1U2F1H-14.6.11-12



ORDERING INFORMATION

Model	Description
5560	SOSA aligned 3U VPX co-processor, Versal HBM ACAP

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