

Flexor 5983-317

8-channel 250 MHz A/D with DDCs
3U VPX board with Kintex UltraScale FPGA

Complete radar and software radio interface solution

- Radar and software radio receiver
- Communications receiver
- Analog signal interface for data recording
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces



Model 5983 is a member of the Flexor® family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot. As an integrated solution, the Model 5983-317 FlexorSet® combines the Model 5983 and the Model 3317 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983's mounted in the same chassis or even over extended distances between them.

Note: There is a 5983A version of this product. See FlexorSet Models.

FEATURES

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx® Kintex® UltraScale FPGA
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB and 5 GB of DDR3 SDRAM
- Sample clock synchronization to [an external system reference](#)
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial inter-board communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: VITA-46, VITA-48, VIA-66.4 and VITA-65 (Open VPX™ System Specification)
- [Ruggedized and conduction-cooled versions available](#)
- Navigator® BSP for software development
- Navigator® FDK for custom IP development

THE FLEXOR ARCHITECTURE

Based on the proven design of the Mercury Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. The Mercury Navigator® FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.

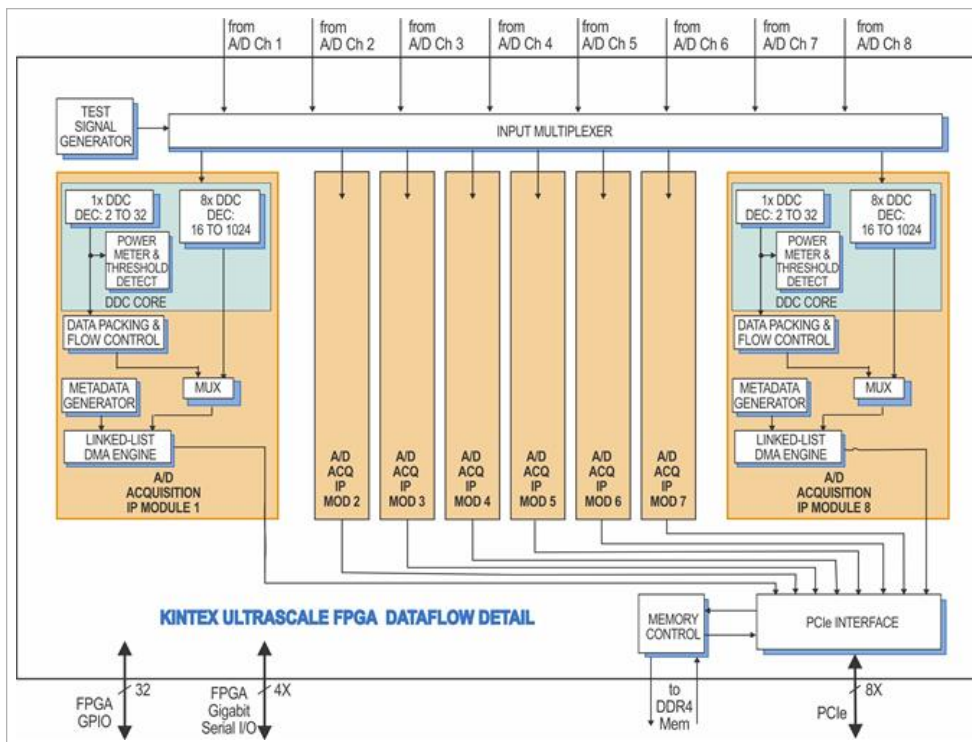
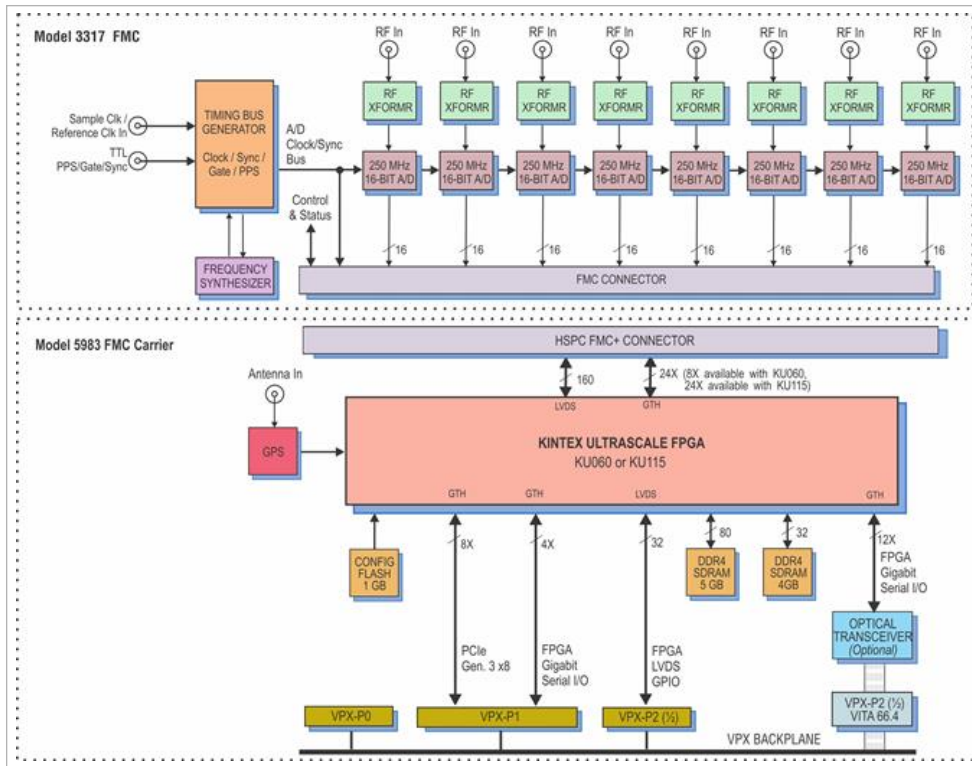
XILINX KINTEX ULTRASCALE FPGA

The 5983-317 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5983-317 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

5983-317 BLOCK DIAGRAM



A/D CONVERTER STAGE

The board's analog interface accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

A/D ACQUISITION IP MODULES

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP CORES

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board.

Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications. The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 * f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N . Each

DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers. In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

CLOCKING AND SYNCHRONIZATION

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

MEMORY RESOURCES

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI EXPRESS INTERFACE

The Model 5983-317 includes an industry-standard interface fully compliant with PCIe Gen. 1, 2 and 3 bus specifications. PCIe links up to x8 are supported.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

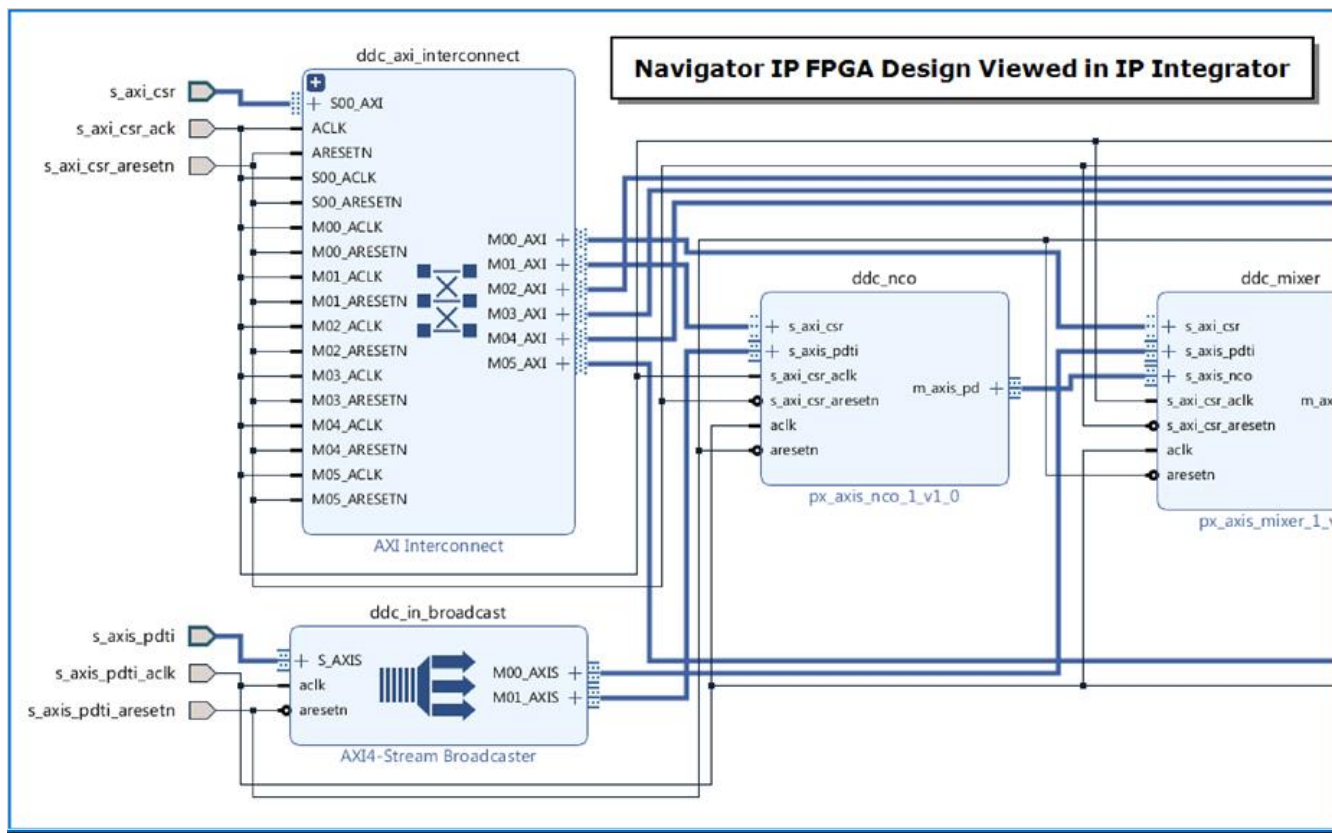
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado’s IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

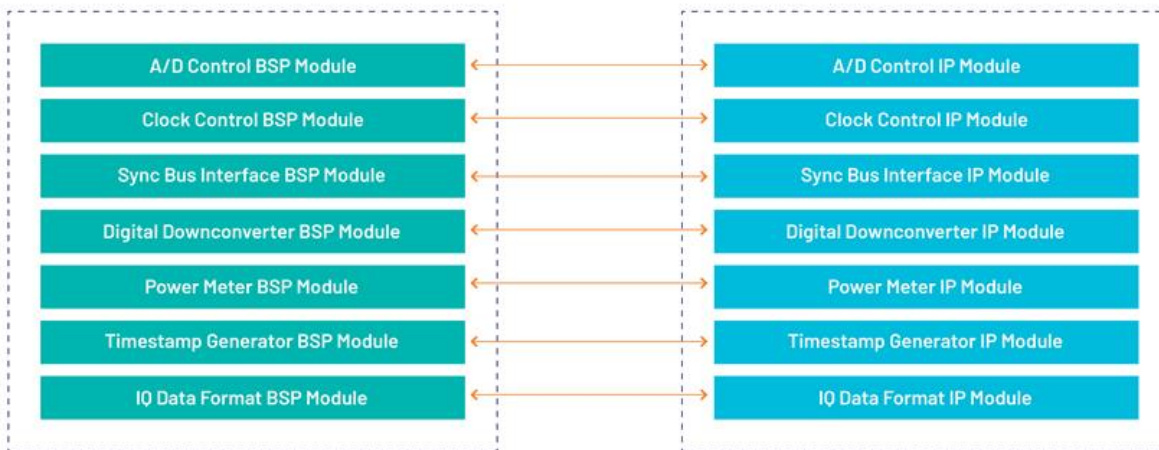
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

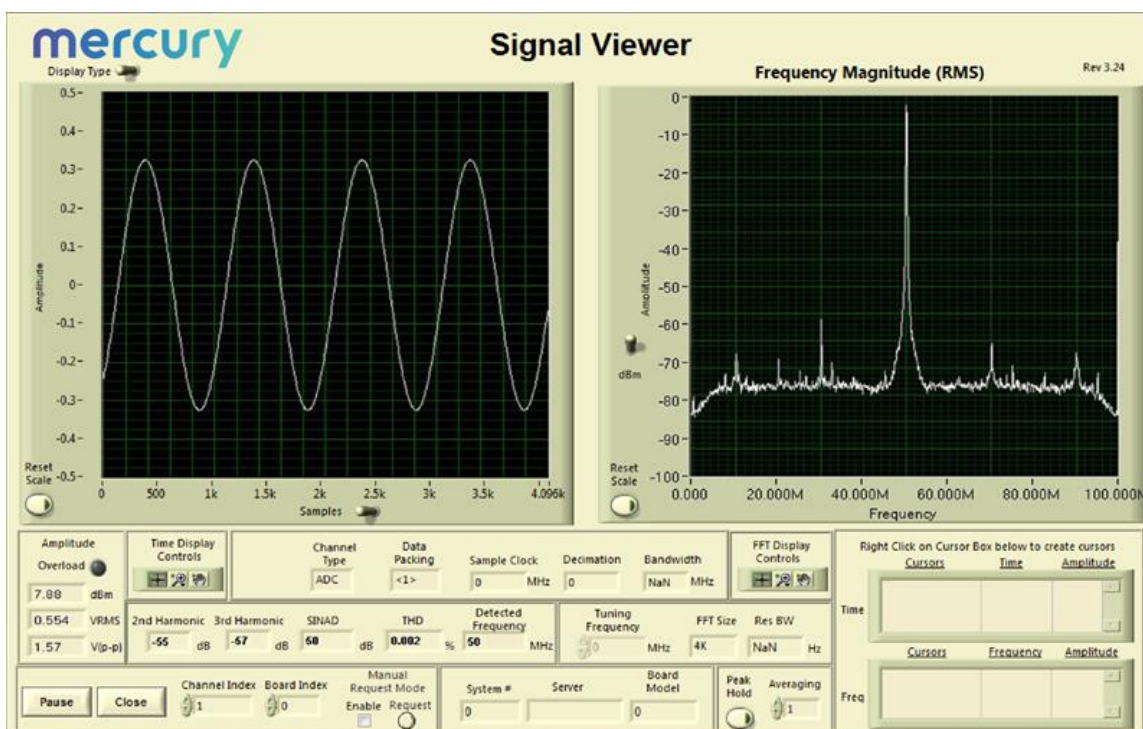
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



FRONT PANEL CONNECTIONS

The FMC front panel includes ten SSMC coaxial connectors for input/output of timing and analog signals. The front panel also includes four LEDs.



- **Analog Input Connectors:** Eight coaxial connectors, labeled **IN 1, 2, 3, 4, 5, 6, 7,** and **8**, one for each ADC input channel. **IN 1** and **2** are input to the first ADS421.B69 and **IN 3** and **4** are input to the second ADS421.B69. to the ADC32RF45.
- **ADC Overload LED:** The red **OV** overload LED indicates an overrange condition in one or more of the eight ADC input channels.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC connector, labeled **CLK** for the input of an external sample clock.

- **User LED:** The green **USR** LED is available for user applications.

Over Temperature LED: The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.

- **Trigger Input Connector:** One SSMC coaxial connector labeled **TRG** for input of an external trigger.

FRONT PANEL CONNECTIONS

The 5983 3U VPX carrier front panel houses the front panel of the FMC installed on the carrier. The carrier front panel includes a reset button, two or four MMCX coaxial connectors, a JTAG connector, and three LED indicators



- **Reset Button:** The white reset button, labeled **RST**, provides a reset and safe reboot of the onboard GPS receiver (Option 180).
- **VPX Clock Connector:** The MMCX connector labeled **VPX CLK** provides output of the 100-MHz PCI clock from the VPX P0 connector (see VPX P0 Utility Connector).
- **10 MHz Reference Connector:** With Option 180, the MMCX connector labeled **REF OUT** provides output of the 10-MHz PCI clock from the onboard GPS receiver.
- **GPS Antenna Connector:** With Option 180, the front panel has one MMCX connector, labeled **GPS ANT**, for input of an antenna RF signal for the onboard GPS receiver. The antenna input signal has a sensitivity of +2 dBm to -167 dBm into 50W input impedance.
- **PPS Connector:** The MMCX connector labeled **PPS** provides output of a PPS signal that can be derived from the onboard GPS receiver (Option 180).

- **PCIe Link LED:** The green **PCIE LNK** LED illuminates when a valid PCIe link has been established over the VPX interface.
- **JTAG Connector:** The carrier front panel provides a 12-pin JTAG connector to download programs and to perform boundary-scan tests on the devices.
- **Over Temperature LED:** The red **TEMP** LED illuminates when an over-temperature or over-voltage condition is indicated by the temperature/voltage sensors.
- **User LED:** The yellow **FPGA USR** LED is available for user applications.

Note: If your 5983 is ordered with Option 763 for mounting in a conduction-cooled VPX chassis, it would have a conduction-cooled VPX Carrier Front Panel.

SPECIFICATIONS

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69

Sampling Rate: 10 MHz to 250 MHz

Resolution: 16 bits

Digital Downconverters

Quantity: Eight channels

Decimation Range: 2x to 32,768x in three stages of 32x

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit user-programmable coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Sample Clock Sources

On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU060-2
- Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O

Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR3 SDRAM

Size: Two banks, one 4 GB and one 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air-cooled)

- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

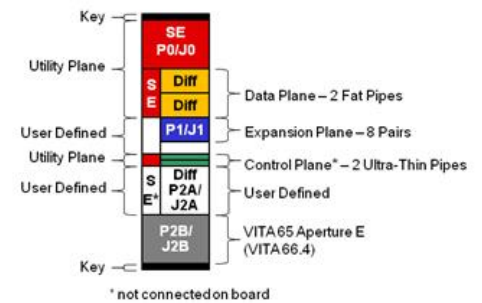
Physical

Dimensions: 3U VPX

- Depth: 100 mm (3.937 in)
- Height: 170.6 mm (6.717 in)

OpenVPX Compatibility

The Model 5983-317 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification: SLT3-PAY-2F1F2U1E-14.6.6-1



FLEXORSET MODELS

This chart shows all available FlexorSets. Click on model numbers for more information.

Form Factor	Software/FPGA Tools	Carrier Model	FMC Model	FlexorSet Model	Description			
3U VPX	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	5973	3312	5973-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A			
				5973-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters			
			3316	5973-316	8-Channel 250 MHz 16-bit A/D			
				5973-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs			
			3320	5973-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A			
			3324	5973-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A			
	KintexUltraScale Navigator BSP Navigator FDK Vivado	5983*	3312	5983-313*	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters			
				5983-317*	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs			
			3320	5983-320*	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A			
			3324	5983-324*	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A			
			PCIe	Virtex-7 ReadyFlow BSP GateFlow FDK Vivado	7070	3312	7070-312	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A
							7070-313	4-Channel 250 MHz A/D & 2-Channel 800 MHz D/A with 4 multiband DDCs & interpolation filters
3316	7070-316	8-Channel 250 MHz 16-bit A/D						
	7070-317	8-Channel 250 MHz 16-bit A/D with 8 multiband DDCs						
3320	7070-320	2-Channel 3 GHz A/D & 2-Channel 2.8 GHz D/A						
3324	7070-324	4-Channel 500 MHz A/D & 4-Channel 2 GHz D/A						

*There is a 5983A version of this product. For differences, see below.

Model 5983	Model 5983A
Flash Memory - 1 Gbit of FLASH Memory	Flash Memory -2 Gbit of BPI FLASH Memory
<p>Optical I/O (Option 110) - VITA 66.4 - Up to 12 duplex optical lanes are available on a VITA 66.4 connector.</p> <p>With the installation of a serial protocol, the VITA 66.4 interface enables a high-bandwidth connection between 5983s mounted in the same chassis or over extended distances.</p>	<p>Optical I/O (Option 110) - VITA 67.3D - Provides 12 duplex lanes @ 10 Gb/sec through the lower half of VPX P2 (VPX P2B).</p> <p>With the installation of a serial protocol, the VITA 67.3D interface enables gigabit communications between boards and chassis, independent of the PCIe interface.</p>
	<p>Custom Analog I/O (Option 113) - VITA 67.3 - VITA 67.3 provides 10 coax connections through the lower half of VPX P2.</p>

DEVELOPMENT SYSTEMS

Mercury offers development systems for Flexor products. They come with all pre-tested software and hardware ready for immediate operation. These systems are intended to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Flexor boards. Please contact Mercury to configure a system that matches your requirements.

ORDERING INFORMATION

Model	Description
5983-317	8-Channel 250 MHz A/D with DDCs and Kintex Ultra Scale FPGA - 3U VPX

Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air-cooled, Level 2
-763	Conduction-cooled, Level 3

Contact Mercury for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Mercury for the latest information.

ACCESSORY PRODUCTS

Model	Description
2171	Cable kit: SSMC to SMA
5292	High-speed synchronizer and distribution board - 3U VPX model
9192	Rackmount high-speed system synchronizer unit

LIFETIME SUPPORT FOR FLEXOR PRODUCTS

Mercury offers worldwide customers shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, and mature software development tools. We offer free lifetime support from our engineering staff, which customers can depend on through phone and email, as well as software updates. Take advantage of our 40 years of experience in delivering high-performance radar, communications, SIGINT, EW, and data acquisition MIL-Aero solutions worldwide.



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