Quartz 6001

8-channel A/D & D/A QuartzXM module with Xilinx Zynq UltraScale+ RFSoC - Gen 1

Unique QuartzXM eXpress Module enables custom deployment

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces

Quartz® Model 6001 is a high-performance Quartz eXpress Module (QuartzXM) based on the Xilinx Zynq UltraScale+ RFSoC FPGA. The RFSoC FPGA integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip.

The 6001 has been designed to bring RFSoC performance to a wide range of different applications by offering the FPGA in a small system-on-module solution measuring only 2.5 by 4 inches. In addition to the RFSoC FPGA, the 6001 includes all of the support circuitry needed to maximize the performance of the RFSoC. The 6001 is available on standard form factor carriers including 3U VPX, SOSA aligned 3U VPX, PCIe, and small form factor enclosures in both commercial and rugged options. In many applications one of Mercury's carrier configurations can provide a final, deployable turn-key solution.

In situations where only a custom form factor will satisfy the application requirements, Mercury supports the 6001 with a design kit that helps users engineer and build their own custom carrier. As a complete and tested module, the Model 6001 QuartzXM encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing users to focus on an application-specific carrier design.

FEATURES

- Unique QuartzXM eXpress Module enables deployment in custom form factors
- Incorporates Xilinx® Zynq® UltraScale+™ RFSoC
- 16 GB of DDR4 SDRAM
- LVDS connections to the Zynq UltraScale+ FPGA for custom I/O
- GTY connections for gigabit serial communication
- Ruggedized and conduction-cooled versions available
- Includes a complete suite of IP functions and example applications
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- Carrier Design Package available to enable custom carrier design
- Free lifetime applications support

BOARD ARCHITECTURE

The 6001 board design positions the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, generation, and processing solutions for many of the most common application requirements. For many applications, the Model 6001's built-in functions can be used as the foundation for custom applications.

EXTENDABLE IP DESIGN

For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 6001's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 6001 either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

CARRIER DESIGN PACKAGE

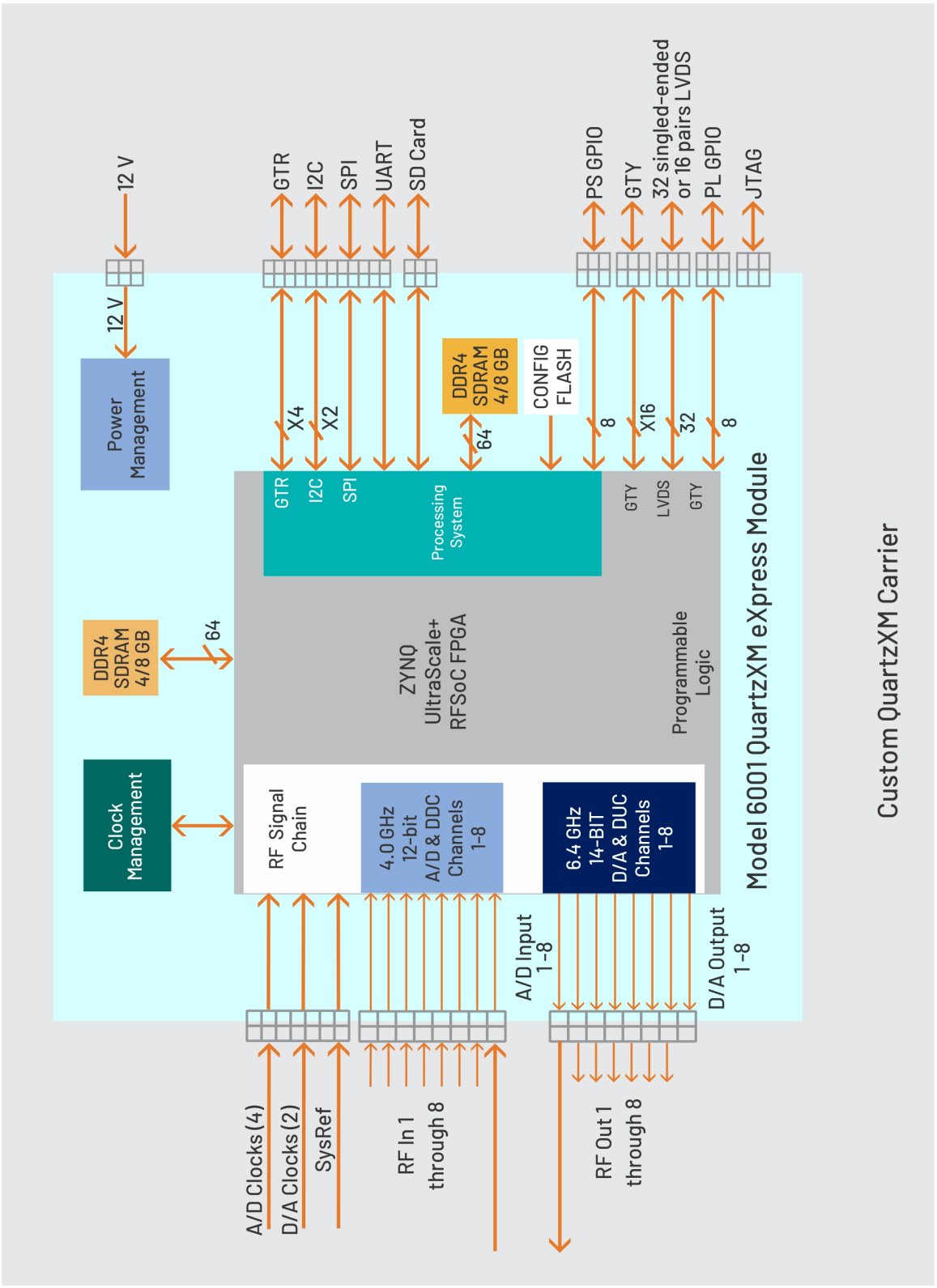
Mercury offers the Model 4801 Carrier Design Kit for users interested in designing their own carrier for the 6001 QuartzXM. The kit uses the Mercury Model 5950 3U OpenVPX carrier as a reference design. The kit includes:

- Pin definitions and electrical specifications of all signals on the module
- 3D models of the module
- Thermal profiles of the module and components
- Carrier reference design schematics
- PCB stack-up recommendations
- PCB design guidelines and routing rules
- Operating system and bootstrap guidelines
- Additional electrical and mechanical engineering guidance

Model 6001 QuartzXM customers must purchase the Model 5950 3U VPX carrier board, which includes the QuartzXM within an open-standard form factor. This allows the user to start IP development and proof of concept designs immediately on a known, tested platform while they develop their own carrier for later deployment. To further speed development tasks, Mercury offers a single-slot 3U VPX development chassis with the Model 5950 installed, along with a rear transition module (RTM) and all needed cables.

6001 BLOCK DIAGRAM

Click on a block for more information.



A/D CONVERTER STAGE

The 6001 accepts analog IF or RF inputs from the carrier board on a multichannel connector, delivering the inputs as differential pairs into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x, or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture, or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A CONVERTER STAGE

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x and 8x. The individual D/A outputs are delivered to the carrier board through a multichannel connector as differential pairs.

When the 6001 QuartzXM is installed on Mercury's 3U Open VPX carrier as the Model 5950, both the RF inputs and outputs are transformer coupled to front panel MMCX connectors. For applications that require special analog processing or connectorization, the 6001 can be mounted on a custom-designed carrier to satisfy the specific application requirements.

CLOCKING AND SYNCHRONIZATION

The 6001 accepts all of the clock signals required by the RFSoC through a multisignal connector from the carrier. In addition, the 6001 design includes a clock management section for distributing the clock and synchronization signals throughout the module.

MEMORY RESOURCES

The 6001 architecture supports up to a 8 GByte bank of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, along with the Mercury-supplied DDR4 controller core within the FPGA, can take advantage of the memory for custom applications.

Up to an 8 GByte bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

PCI EXPRESS INTERFACE

In many applications, the 6001 will be used with a PCIe interface provided by the carrier. The Navigator FDK library includes multiple DMA controllers for efficient transfers to and from the module.

POWER MANAGEMENT

The RFSoC FPGA requires nine different and separate power supplies. In addition, other peripheral circuits needed by the RFSoC require separate supplies. The 6001 includes thirteen different onboard power supplies to support the RFSoC and associated circuitry. Because the supply complexity and sequencing is managed by the 6001 module, a custom carrier needs only to provide a single 12V supply to the module, greatly simplifying the carrier design.

EXPANDABLE I/O

The 6001 provides an interface to all of the digital signals needed by the RFSoC's processing system and programmable logic sections through a high-speed connector to the carrier. The RFSoC's GTY high-speed gigabit serial interfaces are supported by connectors capable of delivering 28 Gb/sec, needed for protocols like 100GigE.

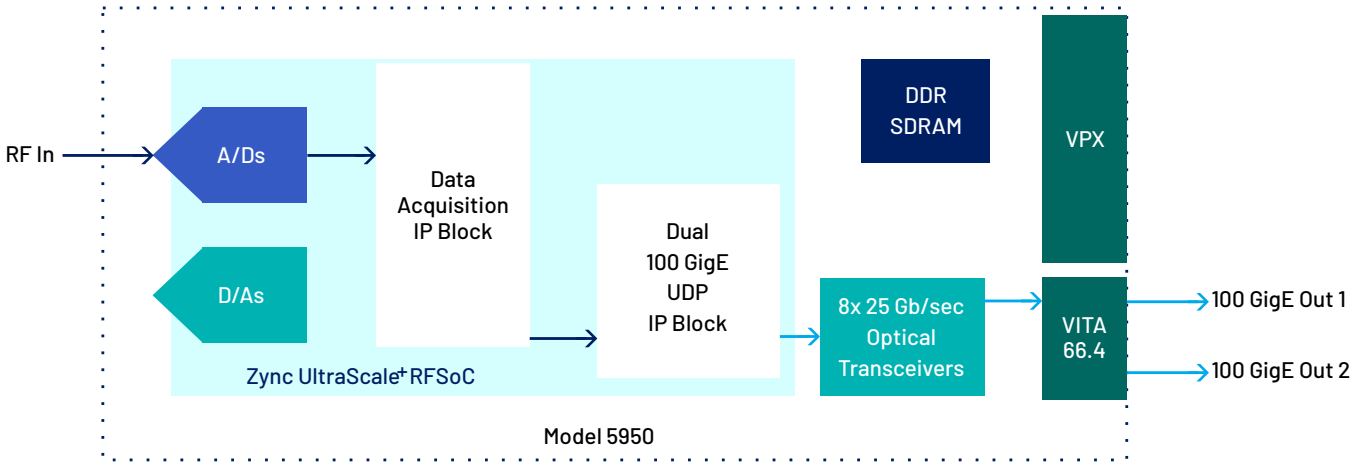
OPTIMIZED IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Mercury helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications.

Several example applications using the Mercury Model 5950 are described on the following pages. (The Mercury Model 5950 delivers the 6001 QuartzXM as a 3U OpenVPX board.) For each example, the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Navigator IP library or for adding custom IP.

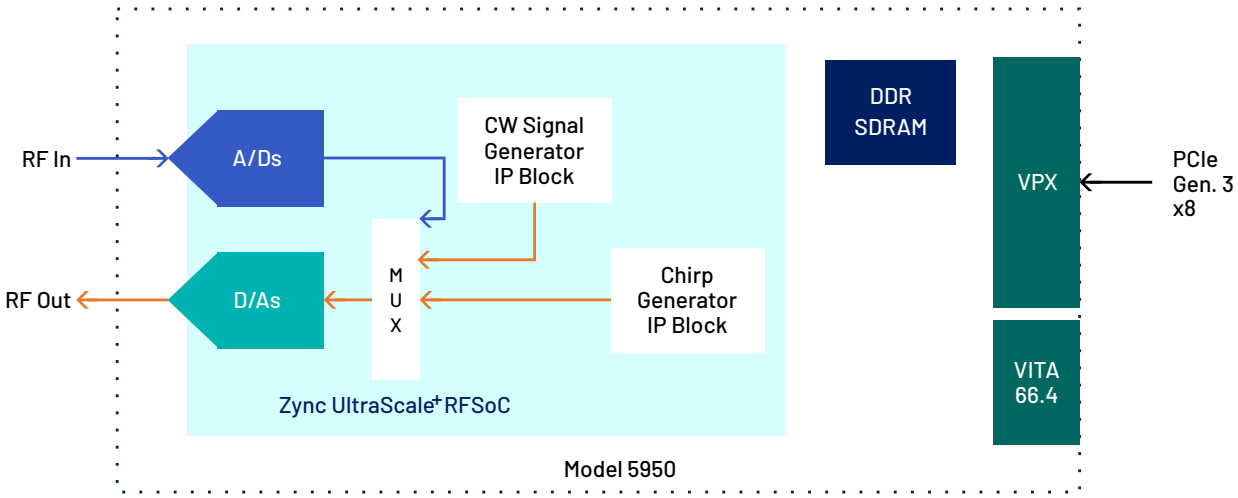
EXAMPLE 1 - HIGH BANDWIDTH DATA STREAMING

The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GB/sec when all channels are enabled. While capturing this much raw data is not feasible, the A/Ds built-in digital downconverters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system. In some applications capturing the raw, full bandwidth data is crucial. The 5950's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board. Along with the built-in data acquisition IP, the 5950 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.



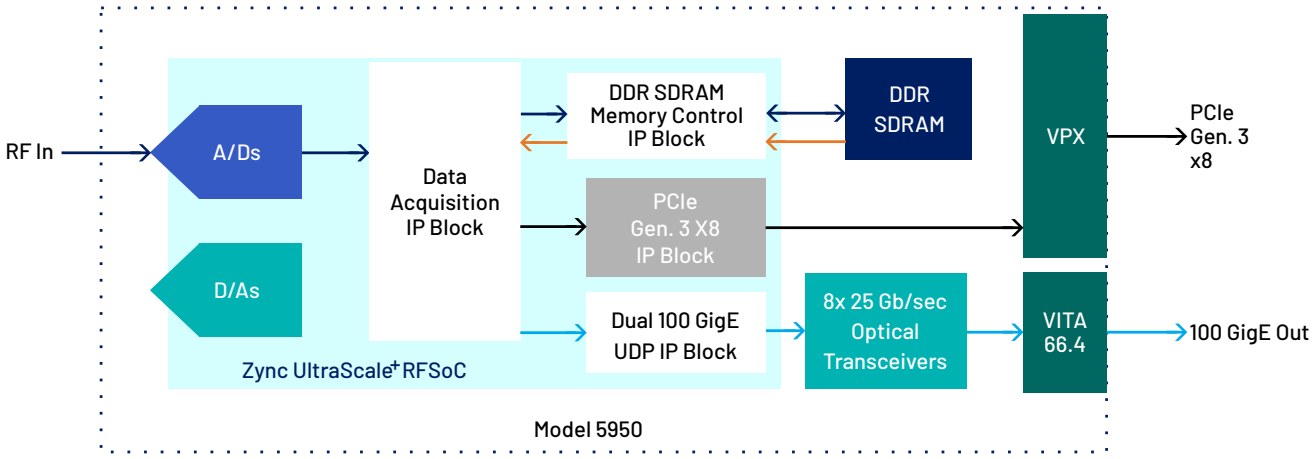
EXAMPLE 2 - WAVEFORM GENERATOR

The 5950's IP supports multiple D/A signal source options. A simple loopback path allows samples received by the A/Ds to be output through the D/As. A CW signal generator produces a sine output with programmable frequency. A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset, and length. The generators also include flexible trigger options with both internal and external triggering.



EXAMPLE 3 - MULTIMODE DATA ACQUISITION SYSTEM

In some applications multiple data acquisition modes may need to be operated at the same time. A required dataflow could be full bandwidth streaming of a single A/D channel over 100 GigE to a data recorder while another channel of A/D data is stored as snapshots in the board's DDR4 SDRAM and read by the ARM processor while yet other A/D channels are down converted using the A/Ds' built-in DDCs and streamed over PCIe. The 5950 provides these modes with built-in IP supporting complex data streaming scenarios without the need for creating custom IP.

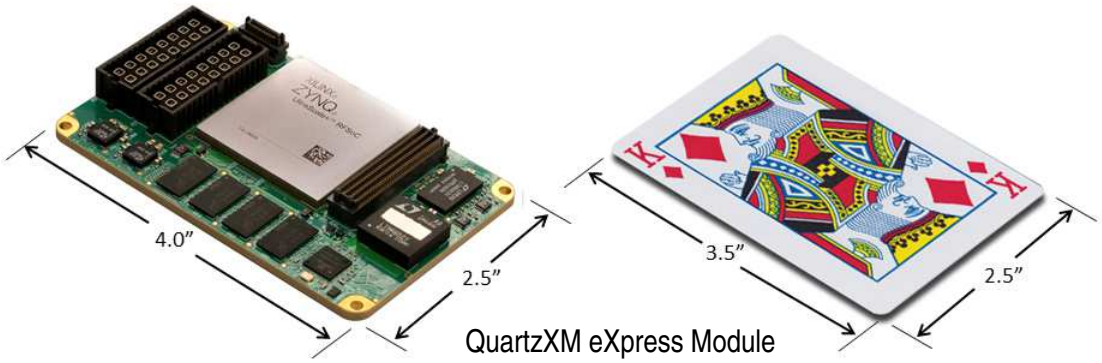


FLEXIBLE MODULAR DESIGN

While the Quartz 6001 follows the form factor of a standard 3U OpenVPX board, the unique modular design of Mercury's 6001 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC FPGA, DDR4 SDRAM, and power and clock management.

In the case of the 6001, the QuartzXM is mounted on a 3U OpenVPX carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver and an 8x 28 Gbps optical transceiver. As a module and carrier board set, the 6001 becomes a complete, ready to deploy 3U OpenVPX solution available for a range of operating environments from commercial to rugged and conduction-cooled.

The 6001 QuartzXM can also be mounted on other carriers available from Mercury to support standard form factors; or for applications that require a non-standard footprint, Mercury supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.



QuartzXM eXpress Module

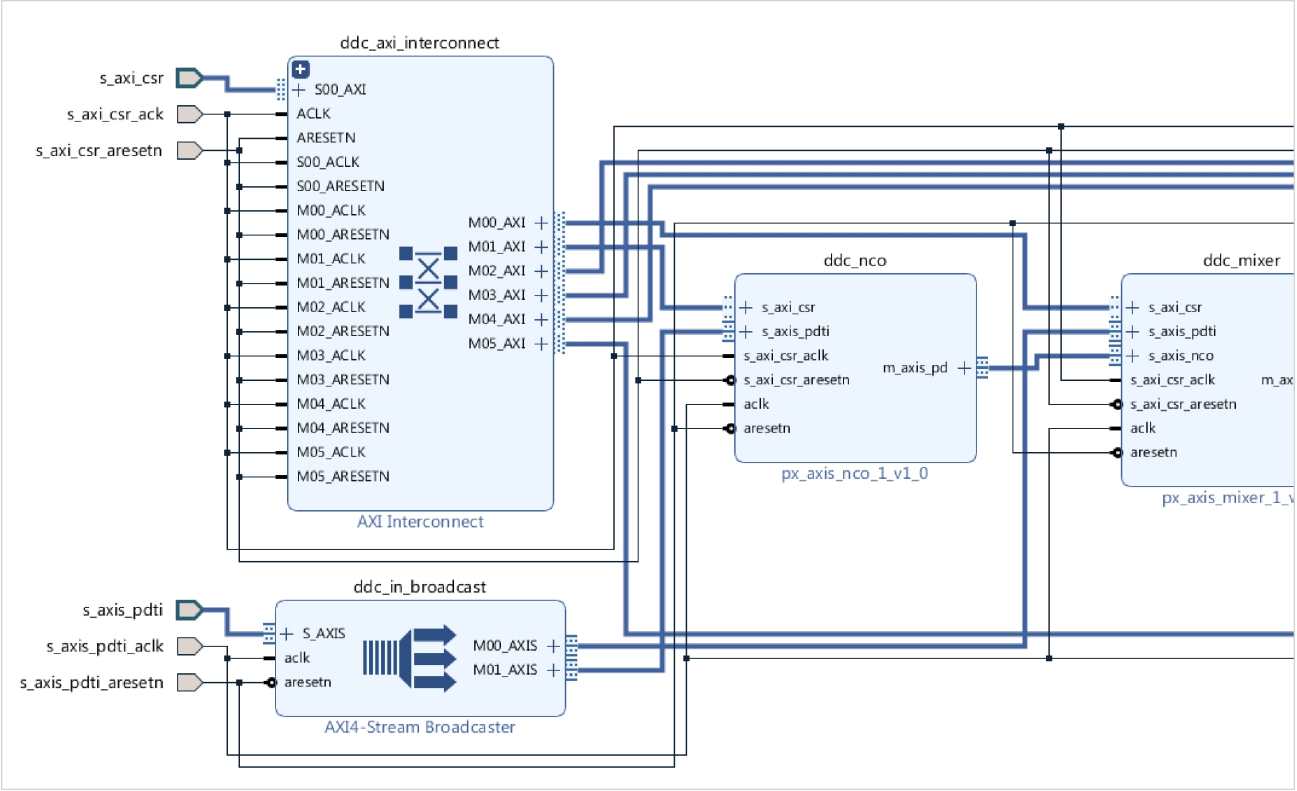
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

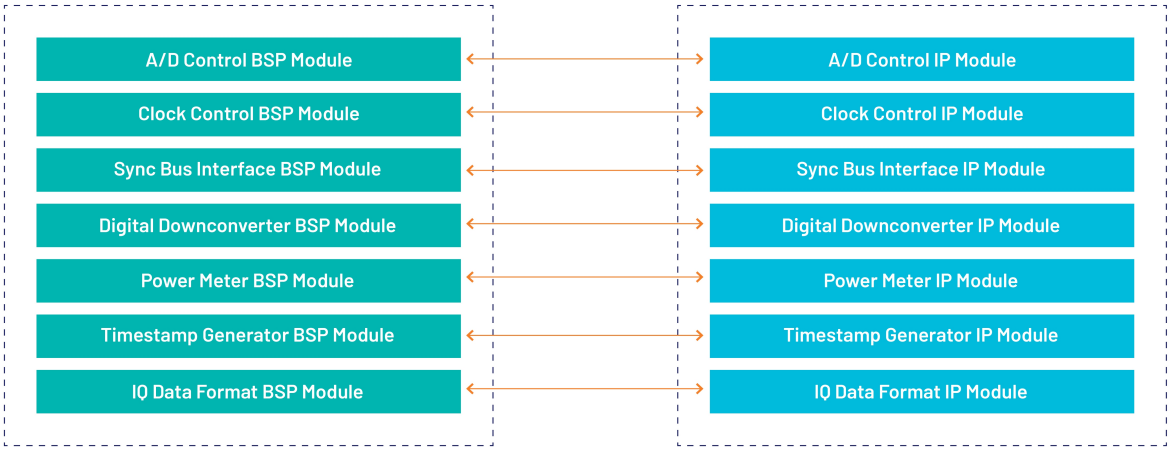
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

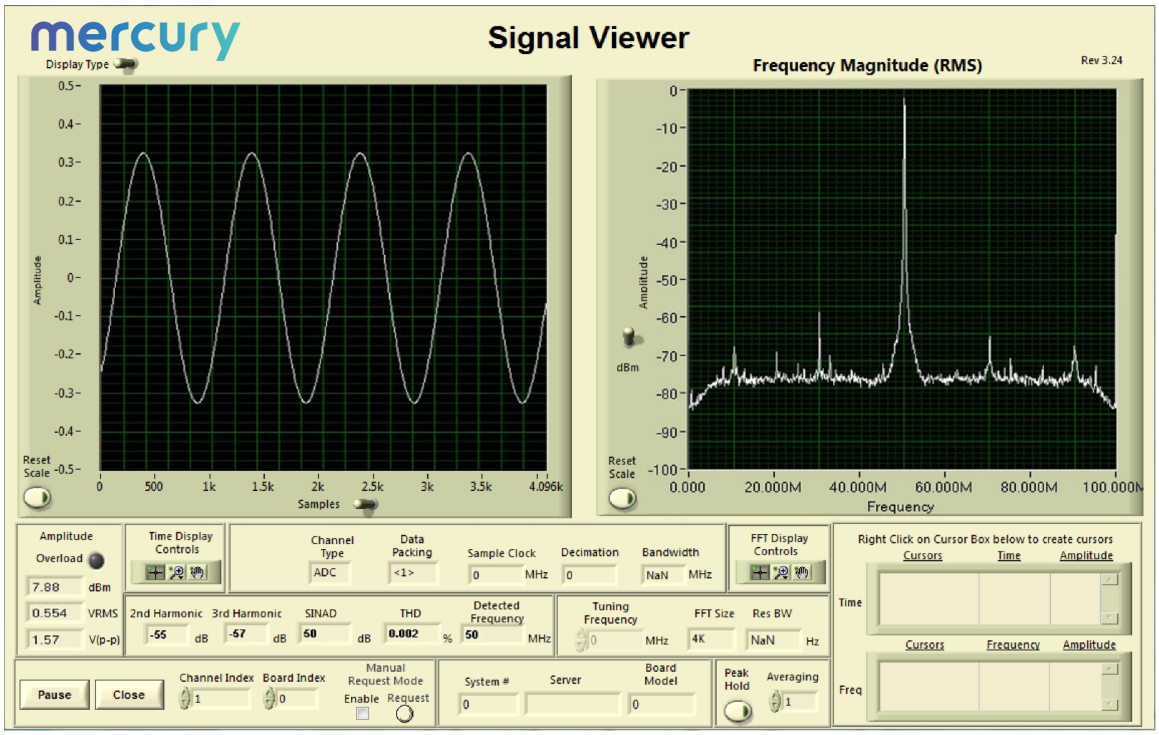
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU27DR

- Option -028: RFSoC XCZU28DR

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs

- Quantity: 8
- Connector: Board-to-board, multichannel differential
- Input Type: Differential
- Full Scale Input: 1Vp-p into 100 ohm on-die termination
- RF Input Frequency Max: 4 GHz (as per Xilinx datasheet)

A/D Converters

- Quantity: 8
- Sampling Rate: 4.0 GHz
- Resolution: 12 bits

Digital Downconverters

- Quantity: 1 per A/D
- Decimation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits, 0 to f_s
- Filter: 80% pass band, 89 dB stop-band attenuation

Analog Outputs

- Quantity: 8
- Connector:Board-to-board, multichannel differential
- Input Type: Differential
- Full Scale Output: 32 mA

D/A Converters

- Quantity: 8
- Sampling Rate: 6.4 GHz
- Resolution: 14 bits

Digital Upconverters

- Quantity: 1 per D/A
- Interpolation Range: 1x, 2x, 4x, and 8x
- LO Tuning Freq. Resolution: 48 bits
- Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock

- Source: Received through board-to-board, multichannel connector
- Quantity: 4 A/D clocks, 2 D/A clocks
- SysRef
- Received through board-to-board, multichannel connector

RFSoC RF Processing System

ARM Cortex-A53:

- Quantity: 4
- Speed: 1.5 GHz

ARM Cortex-R5:

- Quantity: 2
- Speed: 600 MHz

QuartzXM Digital Connector (Programmable Logic)

Parallel: 32 single-ended or 16 pairs of LVDS connections

GTY: 16 full duplex lanes @ 28 Gb/sec Processing

GPIO: 8 single-ended

QuartzXM Digital Connector (Processing System)

GTR: 4 full duplex lanes

I2C: Quantity 2

SPI: Quantity 1

UART: Quantity 1

SD Card Interface: Quantity 1

GPIO: 8 single ended

Memory

Processing System:

- Type: DDR4 SDRAM
- Size: (standard) 4 GB; Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)

Programmable Logic:

- Type: DDR4 SDRAM
- Size: (standard) 5 GB; Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Option -703: L3 (conduction-cooled)

- Operating Temp: –40° to 70° C
- Storage Temp: –50° to 100° C
- Relative Humidity: 0 to 95%, noncondensing

Physical

Dimensions:

- Depth: 101.6 mm (4 in)
- Height: 63.5 mm (2.5 in)

Weight: 3.5 oz (99 grams)

ORDERING INFORMATION

Model	Description
6001	8-channel A/D & D/A QuartzXM module with Xilinx Zynq UltraScale+ RFSoC - Gen 1

Options	Description
-002	-2 FPGA speed grade, -1 standard
-028	XCZU28DR FPGA (XCZU27DR is standard)
-151	8 GB processor system memory, 8 GB programmable logic memory
-703	Air-cooled, Level L3
Contact Mercury for compatible option combinations and complete specifications.	

Model	Description
4801	QuartzXM Carrier Design Kit

QUARTZ PRODUCTS

The 6001 is also available on these carriers:

Model	Description
5550	8-Channel A/D & D/A Zynq UltraScale+ RFSoC (Gen 1) SOSA aligned 3U VPX board
5950	8-Channel A/D & D/A Zynq UltraScale+ RFSoC (Gen 1) 3U VPX board
6350	8-Channel A/D & D/A Zynq UltraScale+ RFSoC (Gen 1) small form factor enclosure
6350S	8-Channel A/D & D/A Zynq UltraScale+ RFSoC (Gen 1) small form factor subsystem
7050	8-Channel A/D & D/A Zynq UltraScale+ RFSoC (Gen 1) PCIe board

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP6001

For technical details, contact:
mrcy.com/go/CF6001