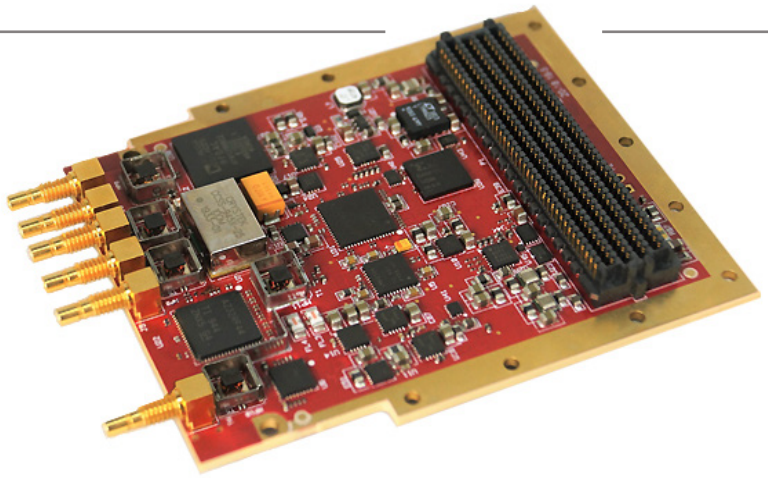


FMC165 FPGA Mezzanine Card

Dual Channel ADC and Single Channel DAC

The FMC165 provides two 14-bit analog-to-digital (A/D) channels supporting RF sampling at 2.6 GSPS and one 14-bit digital-to-analog (D/A) channel with sampling rates up to 5.2 GSPS (2.6 GSPS direct RF synthesis). The converters are clocked by either an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. In addition, a trigger input for customized sampling control is available to users.

The FMC165 daughter card is mechanically and electrically compliant with the FMC standard (ANSI/VITA 57.1). It has front panel I/O and can be used on any FMC/FMC+ compatible carrier in an air-cooled configuration. In a conduction-cooled environment, it can be used with Abaco FPGA carrier cards.

The design is based on Texas Instruments' high-speed, high-performance ADC32RF44 A/D converter (ADC) and Analog Devices' AD9129 D/A converter (DAC). The analog signals are AC coupled connecting to SSMB coax connectors on the front panel.

The FMC165 allows flexible control of clock source through serial communication buses. The card is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions in order to reduce system level power consumption.

The FMC165 is well suited for low power applications such as airborne where the highest level of performance is required while ensuring that mission range is not affected.

FEATURES:

- ADC32RF44 ADC: dual-channel 14-bit up to 2.6 GSPS with DDC (or 14-bit @ 2.5 GSPS with full data rate)
- AD9129 DAC: single-channel 14-bit up to 5.2 GSPS (2.6 GSPS data rate)
- RF input bandwidth up to 3.2 GHz and output up to 2.6 GHz in x2 interpolation mode
- JESD204B (A/D), LVDS (D/A) FPGA data buses
- Single-ended AC-coupled analog signals
- 6 SSMB connectors available from the front panel
- Clock source, sampling frequency and calibration through I2C communication
- buses
- Flexible clock tree enables
  - on board VCO - 1.5 to 2.6 GHz
  - external reference clock
  - external sampling clock
- Multi-board synchronization capable
- ANSI/VITA 57.1 compliant
- HPC (high pin count) compatible
- Conduction-cooled configuration available on Abaco FPGA carrier cards

abaco SYSTEMS

FMC165 FPGA Mezzanine Card Dual Channel ADC and Single Channel DAC

Operating Temperature

- 0°C to +55°C (air-cooled environment with 400 LFM mean airflow)
- -40°C to +75°C (conduction-cooled environment at the card thermal interface)

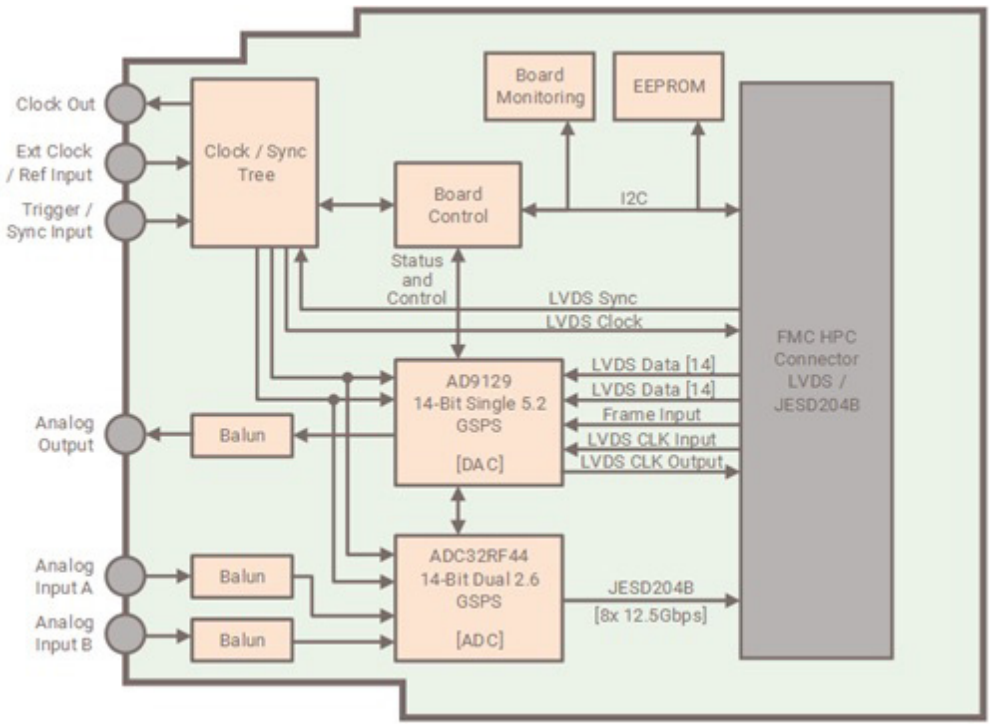
Applications

- Direct RF down conversion
- Electronic warfare (EW)
- Radar/Sonar
- Software defined radio (SDR)
- Ultra-wide-band satellite digital receiver
- Medical equipment
- Aerospace and test instrumentation

Support

- StellarIP and compatible reference designs are available for this product; StellarIP provides a simple way to design FPGA firmware with automated code
- Xilinx IP Integrator reference designs available for selected FPGA carrier cards
- Windows® and Linux® (for VxWorks® support contact factory)
- User manual
- Performance report
- Support provided on Abaco Systems private support forum

Block diagram



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Americas: 866-OK-ABACO or +1-866-652-2226

Europe, Africa, Middle East, & Asia Pacific: +44 (0) 1327-359444

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