DELPHI ENGINEERING GROUP

DATASHEET

ADF-3000/2600

3.0/2.6 Gsps, 10 Bit, ADC FMC Module

BENEFITS

- High Sample Rate, High Resolution
- SWaP-C Applications
- VITA 57.1 R2010 Compliant
- Rugged and Reliable

FEATURES

- 3.0/2.6Gsps, 10-bit ADC
- 100KHz to 5GHz input bandwidth
- FMC form factor
- Air and Conduction-Cooled

PERFORMANCE

- 500 Msps to 3.0Gsps sampling rate
- 2.6Gsps Option Available
- ENOB: 7.8 Effective Bits@ FIN = 1245MHz
- SNR: 44dBFS@ FIN = 1245MHz
- SFDR: 49dBFDR@ FIN=1245MHz

The ADF-3000 reaffirms DEG's leadership position in the high speed, high performance analog to digital conversion market. By leveraging previous ADC card designs and using E2V's highest performance A/D converter, Delphi engineers have created an FMC card that leads the industry in both resolution and dynamic performance. This FPGA Mezzanine Card (FMC) converts a single channel up to 5GHz analog input bandwidth at 3.0Gsps and 10-bit resolution. Based on the VITA 57 specification, the ADF-3000 enables direct coupling of unparalleled analog-digital conversion capability with the VME/VXS/AMC/VPX/PCI-E carrier board of your choice.

The ADF-3000 is based on E2V's latest innovation, the EV10S152, which sets the benchmark for high performance analog to digital conversion. DEG engineers leveraged design work and intellectual property from the highly successful ADF-2500 FMC module. By coupling this core architecture with the compact and flexible FMC form factor, DEG has enabled customers to rapidly and cost-effectively integrate the latest generation of analog to digital conversion capability with very high performance processor/carrier boards. This flexible approach reduces overall power consumption, footprint and cost while increasing ruggedness and reliability.

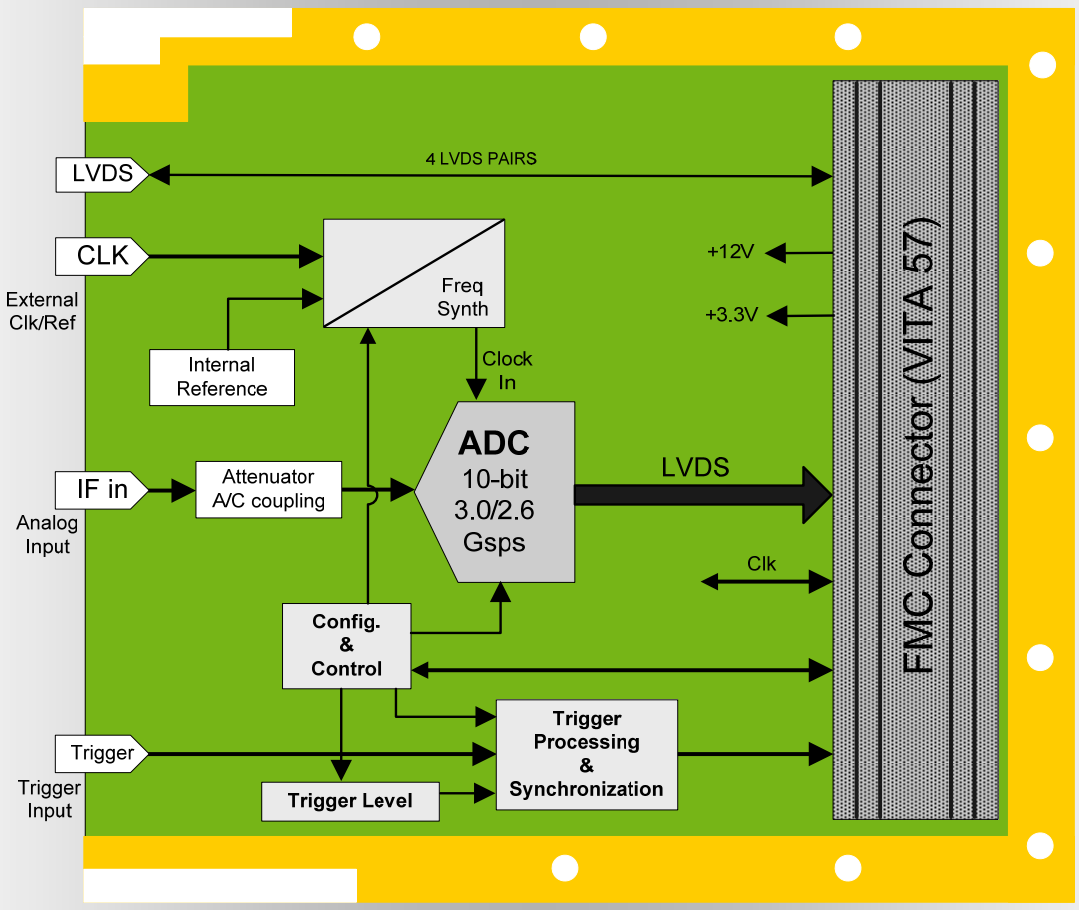
Also available with the ADF-3000/2600 is Delphi's FMC to FPGA VHDL interface logic, ADCLink. ADCLink leverages Delphi's expertise in developing high-speed interfaces between Gsps ADCs and DACs and the latest in rich IO FPGA technology. Fully tested and proven to support multi-GByte transfer rates between FMC and FPGA, ADCLink enables faster digital receiver design times with increased performance capability.

ADF-3000/2600 Performance Specification

Clock and Trigger Specifications	
Connectors	SMA Front Panel
Clock input	50 Ω, AC-coupled
Clock input frequency	500 - 3000 MHz
Internal Reference Clock	1ppm Accuracy
External Reference Clock	10MHz
Std PLL frequency	500 - 3000 MHz
Trigger input	Single-ended 50 Ω

Environmental Specifications	Commercial	Rugged	Conduction-Cooled
Operating temperature	0°C to +50°C (inlet air)	-40°C to +71°C (inlet air)	-40°C to +71°C (card edge)
Storage temperature	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C
Humidity (non-condensing)	0 to 95%	0 to 100%	0 to 100%
Vibration (random)	0.01g^2/Hz, 15-2,000 Hz	0.04g^2/Hz, 15-2,000 Hz	0.04g^2/Hz, 15-2,000 Hz
Shock	20 g peak	30 g peak	40 g peak

- Based on MIL-STD-810F



About DEG

The Delphi Engineering Group (DEG) provides a full range of high-performance COTS-based and customized digital receiver technology, products, and services for mission-critical applications in the aerospace, defense, and communications industries.