DEG
A Signal of Greater Interest

ADF-Q25

Quad 250Msps, 16-bit ADC Receiver

Real Time, High Performance Acquisition Solutions

Overview

The ADF-Q25 is DEG's fastest 16-bit ADC, FPGA mezzanine card (FMC) module. By compressing four 250Msps, 16-bit ADCs onto an FMC, DEG continues to deliver the widest range of high performance, high density FMC ADC modules to the embeded computing marketplace. Based on VITA 57 specifications, the ADF-Q25 enables direct coupling of unparalleled analog-to-digital conversion performance with the VME/VXS/AMC/VPX/PCI-E FPGA carrier of your choice. DEG has designed this product and associated HDL firmware to work with both Xilinx and Altera FPGAs.

The ADF-Q25 is based on the Analog Devices AD9467, analog-to-digital converter and emerging FMC form factor. The ADF-Q25 design and flexible configuration options, enable system designers to rapidly and cost-effectively build compact and rugged systems with up to eight, high-resolution channels on a single high performance processor board. This flexible approach reduces overall power consumption, footprint and cost, while increasing ruggedness and reliability.

Features

- Four 250Msps, 16-bit ADC's
- 900MHz Full Power Input B/W
- FMC/VITA 57 Form Factor
- Air and Conduction-Cooled

Benefits

- Extremely Dense Digitization
- Works with Altera & Xilinx FPGA's
- Industry Standard Form Factor
- Rugged and Reliable

Performance

- 50Msps to 250Msps
- 900 Mhz Input Bandwidth
- 12.1 ENOB, Fin = 140Mhz
- 8 Channels in Single VXS/VPX Slot

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ADF-Q25 Details

The front panel of the ADF-Q25 has a micro-connector CMM220 and an HDMI connector. The micro-connector supports six 50Ω connections. A breakout cable converts the micro-connector ports to male SMA connectors. These connectors provide 4 analog inputs, A/D sampling clock/external reference clock input, and trigger input. The front panel HDMI connector supports four uncommitted differential connections with the host (LVDS or other). Data rate up to 5Gsps supported.

Analog Input

The analog input is single-ended with a full-scale of 1.84Vpp. The analog input signal bandwidth extends up to 300MHz and depends on FMC version. See Table.

Clocks

The user can provide a sampling clock to A/D converters or use the onboard frequency synthesizer to provide the clock. The clock input is designed to accept either an external sampling clock signal or external reference for the on-board synthesizer. Functionality of the input is set by the user. The frequency synthesizer can be locked to an on-board reference or an external one provided through the clock input connector. Reference input from the FMC connector is also supported. The reference input must be a sine or square (preferred) wave, with an amplitude range of 0dBm to +10dBm. Several output frequencies predefined from the onboard synthesizer, see Table. Custom values can be synthesized as well.

Triggers

Trigger input must be 200mV to 2V p-p signal Rise time of less than 10 ns is recommended. A trigger event is initiated by a positive transition on the trigger signal. An auto-trigger function enables signal capture without an external trigger. A user can set the trigger threshold within a wide range, with 1mV resolution. See Table.

ADCLink

FMC modules are distinct and separate from the FPGA devices that support them. Initiation and control of the ADF-Q25 is accomplished with ADCLink. Board support packages are required for each unique host card.The capabilities of ADCLink include: onboard/ external reference/external clock selection, internal sampling frequency, trigger threshold.

ADF-Q25 Performance Specifications

Analog Specification	Assembly
Number of Channels	4
Input Impedance	50Ω, AC-coupled
Input Bandwidth	1MHz - 150MHz (Version 20) 150 MHz - 300MHz (Version 21)
Full Scale Input	1.84 Vp-p, 12.3dBm max 17.6 dBm damage level
Sampling Clock Range	50MHz - 250MHz
Onboard Reference	Initial calibration ±1ppm Stability ±0.5ppm
External Reference	Square (preferred) or Sine waveform Level 0dBm to 10dBm Frequency 10MHz *N, N=1, 2..., 10 Phase noise level <155dBc/Hz,100Mhz,
Onboard Frequency Synthesizer	Output frequencies 50MHz,100MHz 150MHz, 200MHz, 250MHz
Trigger Input	Square (preferred) or Sine waveform Range 0.2V - 2Vp-p
Trigger Threshold	Range (-2.048)V - +2.048V Resolution 1mV

Product Selection Guide

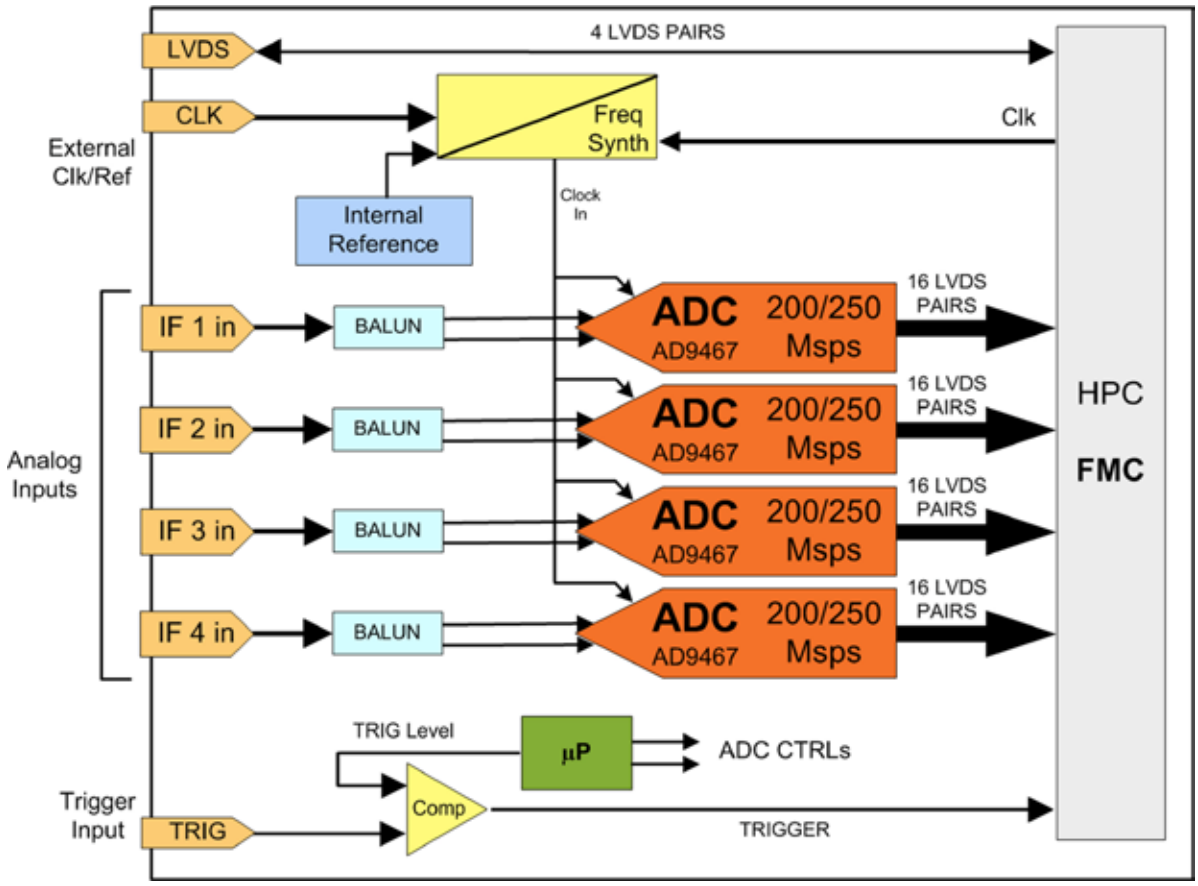
Part Number	Coupling	Rugged Level	Commercial	Rugged	Conduction Cooled	Conformal Coated
ADF-Q25	AC	Commercial	√	-	-	-
ADF-Q25-C	AC	Commercial	√	-	-	√
ADF-Q25-R	AC	Rugged	-	√	-	-
ADF-Q25-RC	AC	Rugged	-	√	-	√
ADF-Q25-CC	AC	Conduction	-	-	√	-
ADF-Q25-CCC	AC	Conduction	-	-	√	√

ADF-Q25 Environmentals

Environmental Specifications	Commercial	Rugged	Conduction Cooled
Operating Temperature	0ºC to +50ºC (inlet air)	-40ºC to +71ºC (inlet air)	-40ºC to +71ºC (inlet air)
Storage Temperature	-55ºC to +85ºC	-55ºC to +125ºC	-55ºC to +125ºC
Humidity (non-condensing)	0 to 95%	0 to 100%	0 to 100%
Vibration (Random)	$0.01g^2$/Hz 15-2,000Hz	$0.04g^2$/Hz 15-2,000Hz	$0.1g^2$/Hz 15-2,000Hz
Shock	20g peak	30g peak	40g peak

Notes: Based on Mil-Spec 810F

ADF-Q25 Block Diagram



For more information or details, please contact:

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