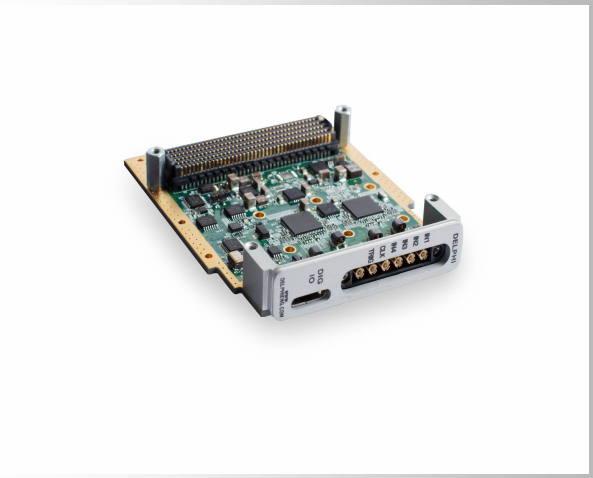


# *ADF-Q3114*

## Quad 3.1 Gsps, 14-bit ADC FMC+
## JESD204B Interface

The ADF-Q3114 ADC FMC module from DEG delivers four channels, each with 14 bits of resolution at sample rates of up to 3.1 Gsps. Utilizing the Analog Devices AD9208 ADC, the ADF-Q3114 enables defense applications requiring higher dynamic range, greater ENOB and wideband sampling performance.

The ADF-Q3114 is a VITA 57.4 compliant FPGA Mezzanine Card (FMC+) that converts four channels of up to 3.0 GHz analog input bandwidth. This digitizer provides unparalleled analog-to-digital conversion capability with the PCIe/VME/VXS/VPX carrier board of your choice. The ADF-Q3114 is designed to be compatible with Xilinx® FPGA platforms.

### *BENEFITS*

- 14 Bit Resolution
- High-speed SERDES interface for multi-Gigabyte IO throughput to host FPGAs
- Wide Dynamic Range
- Convection and Conduction-Cooled Versions

### *FEATURES*

- Quad channel 3.1 Gsps 14-bit ADC
- JESD204B SERDES Interface: x16 Lanes
- Designed for VITA 57.4 compliant FMC + Carrier Boards: Kintex UltraScale & Virtex 7 FPGAs
- Four internal digital down-converters per channel

### *PERFORMANCE*

- 2.5 Gsps to 3.1 Gsps sampling rate

(Other sample rate options available)

- Up to 3 GHz of usable analog input full power bandwidth – AC Coupled.
- ENOB = 9.5 effective bits, $F_{in}$ = 765 MHz
- SNR = 60 dB @ $F_{in}$ = 765 MHz
- SFDR = 71 dB @ $F_{in}$ = 765 MHz

### Flexible, cost-effective solution

By coupling this core architecture with the compact and flexible FMC form factor, DEG enables customers to rapidly and cost-effectively build highly integrated, rugged systems of high-speed digitization in a single FPGA carrier board slot.

The front panel of the ADF-Q3114 provides six coaxial connections that serve as inputs for analog sources, trigger, and clock or external reference.

### ADCLink

DEG offers ADCLink, a custom VHDL interface that provides the SERDES, trigger, and control code specifically for the ADF-Q3114. The capabilities of ADCLink include clock phase adjustment, onboard/external reference clock control, trigger input and thresholds, sampling delay, and ADC mode control.

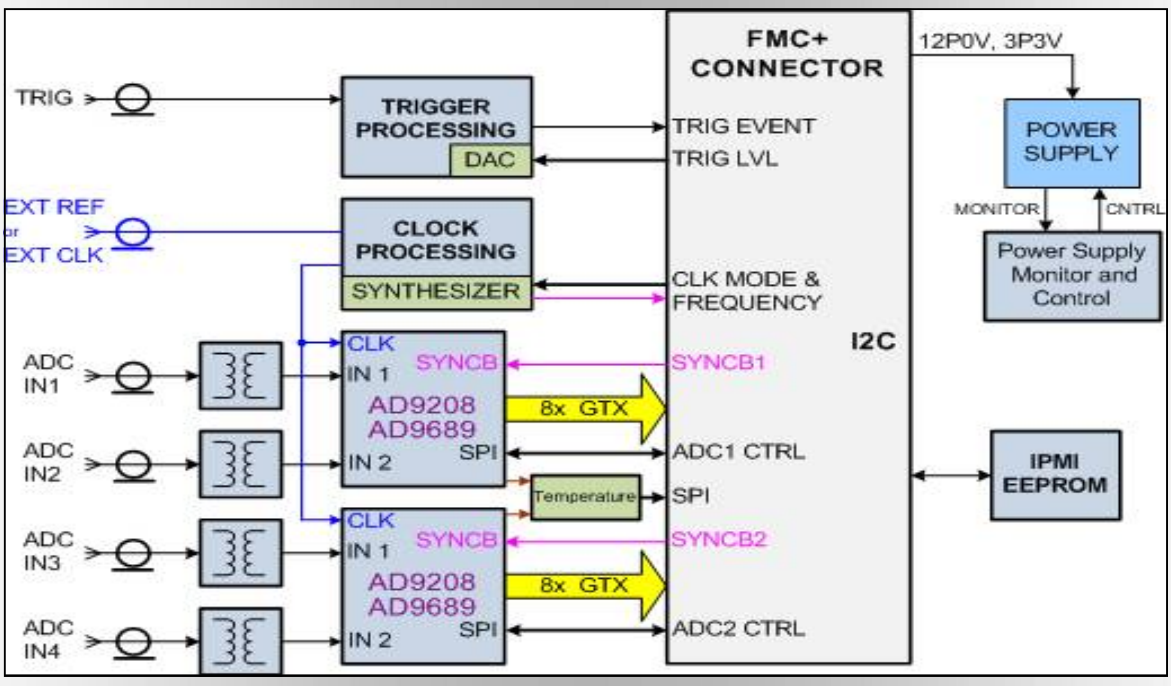
Board support packages are available for each unique DEG host card.

## *ADF-Q3114 Performance Specification*

| Analog Specifications | |
|---|---|
| Number of Channels | 4 |
| Sample Rate Options | 2500 to 3100 Msps,<br>1900 to 2600 Msps<br>1300 to 2100 Msps |
| Input Bandwidth | 3.0 GHz |
| Input Impedance | 50 Ω |
| Maximum Input | 4.3 Vpp |
| SNR (typical*) | 60 dB @ $F_{in}$ = 765 MHz |
| SFDR (typical*) | 71 dB @ $F_{in}$ = 765 MHz |
| ENOB (typical*) | 9.5 eff bits @ $F_{in}$ = 765 MHz |

| Clock and Trigger Specifications | |
|---|---|
| Connectors | 50 Ω |
| Ext Clock Input Frequency | 1300 to 3100 MHz (ADC Specific) |
| Internal Clock Frequency | 20 ppm Accuracy Over Temp |
| External Reference Clock | 10 MHz |
| Trigger Input | Single-ended 50 Ω, DC |
| External Reference | Sine or Square Wave |
| Ext. Ref. Input Amplitude | 200 mVpp to 3 Vpp |

* Typical parameter as supplied by Analog Devices component datasheet




**About DEG**

Delphi Engineering Group (DEG) provides a full range of high-performance COTS-based and customized digital receiver technology, products, and services for mission-critical applications in the aerospace, defense, and communications industries.