



## Applications

- Digital Signal Processing
- Radar/Sonar Beamforming
- ELINT
- Image/Video Processing
- Data Encryption

## Board Features

- Separate PCI Express Bridge FPGA
- High-density FMC Interface
- 2GByte on-board DDR3-1600 SDRAM

## FPGA Features

- 3x PCIe® Gen2 (690T 2x Gen3)

## Summary

The **ADM-VPX3-7V2** is a high performance reconfigurable 3U OpenVPX format board based on the Xilinx Virtex-7 range of Platform FPGAs.

Features include PCI Express Gen2 interface, external memory, high density I/O using a Vita 57 standard, high Pin Count FMC interface, Gigabit Ethernet Interface, system monitoring and flash boot facilities.

A comprehensive cross platform API with support for **Microsoft Windows, Linux and VxWorks** provides access to the full functionality of these hardware features.

Placing the PCI Express bridge in bypass allows the creation of a Gen 2 x8 PCI Express endpoint design directly into the target FPGA (Target FPGAs VX330T and VX690T can also support Gen3 x8 PCI Express designs).

The **ADM-VPX3-7V2** is available in a cost reduced form without a separate Bridge FPGA for high-volume production orders. A Rear Transition Module (RTM) is available to accelerate development by providing monitor and control access to all Rear (backplane) IO signals.



## Target Devices

Xilinx Virtex-7: XC7V585T  
(FF(G)1761)

## FPGA Specification

LUTs = 582k  
FFs = 728k  
DSPs = 1260  
BRAM = 28.6Mb  
3x PCIe® Gen2 (690T 2x Gen3)

## Application Data Memory

4x SDRAM 512MB DDR3-1600

## FPGA Configuration Memory

BPI 512MBit Flash Memory  
Configured as 2x Bridge

## FPGA Configuration Modes

PCI Express direct to SelectMAP port  
From Flash direct on power up  
External JTAG connector

## Deliverables

ADM-VPX3-7V2 Board  
One Year Warranty  
One Year Technical Support

## Host Interface

PCI Express Gen2 x1, x2 or x4 link to separate bridge device with 2GB/s local link to user FPGA  
4 DMA Controllers  
Interrupt Controller

## Board Format

3U VPX (OpenVPX Compliant)

## Input/Output Interfaces

80 Pairsx GPIO

10x High-Speed Serial Links

10x High-Speed Serial Links (compliant to VITA 46.9 X24S+X12D+X8D)

32x GPIO (compliant to VITA 46.9 X24S+X12D+X8D)

**Support**

Comprehensive Software Development Kit with source code for example software and FPGA designs.

**Environmental Specification**
**Temperature Ranges**

Cooling Option	Operating Temperatures		Storage Temperatures	
	Min	Max	Min	Max
AC0	0°C	55°C	-40°C	85°C
ACE	0°C	70°C	-55°C	100°C
AC1	-40°C	70°C	-55°C	100°C
CC0	0°C	55°C	-40°C	85°C
CCE	0°C	70°C	-55°C	100°C
CC1	-40°C	70°C	-55°C	100°C

Operating Humidity : Up to 95% (non-condensing)

**EMC Standards**

FCC 47CFR Part 2  
 EN55022:2010 Equipment ClassB  
 EN55024:2010  
 EN60950-1:2006 (+A12:2011)

**Conformal Coating Options**

Acrylic or Polyurethane  
 Contact sales for specification of coatings.

**Ordering Information**

**Order Code: ADM-VPX3-7V2/z-y(m)(c)(a)**

Option	Code	Description of Options
Vertex-7 device	z	V585T=XC7V585T, VX690T=XC7VX690T
Vertex-7 speed	y	1, 2, 2G, 2L, 3
Memory	m	blank = 2GBytes on board SDRAM (Four banks of 512MBytes), J4 = 4GByte on board SDRAM (Four banks of 1GByte)
Cooling	c	blank = air cooled commercial, /ACE = air cooled extended, /AC1 = air cooled industrial, /CC0 = conduction cooled Commercial, /CCE = conduction cooled Extended, /CC1 = conduction cooled industrial
Conformal Coating	a	blank = no conformal coating, A = Acrylic, P = Polyurethane
Note		not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.

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