General Standards Corporation

High Performance Bus Interface Solutions

CCVPX-16AISS8AO4C

16-Bit, 12-Channel, 2-MSPS Conduction-Cooled 3U VPX Analog Input/Output Board

With Eight Simultaneously Sampled Analog Inputs, Four Analog Outputs, and Input Sampling Rates to 2.0 MSPS per channel

Features

- **Analog Inputs:**
  - 8 Differential analog inputs with dedicated 16-Bit ADC per channel
  - True simultaneous sampling of all inputs to 2.0 MSPS per channel
  - SAR architecture; no minimum sample rate
- **Analog Outputs:**
  - 4 Single-ended analog outputs with dedicated 16-Bit DAC per channel
  - Simultaneous output clocking rates to 1.0 MSPS per channel
  - Selectable direct-write or FIFO-buffered access
  - Buffer configurable as open for data streaming, or circular for periodic functions
- **Common Analog I/O Features:**
  - Selectable input/output ranges: ±10V, ±5V, ±2.5V
  - Independent 256-Ksample input and output FIFO data buffers
  - Hardware clock and sync I/O for multiboard operation
  - Internal power conversion
  - DMA engine minimizes bus congestion
  - Timing controlled by internal rate generator, by software clocking, or externally
  - Three independent 24-Bit frequency dividers
  - On-demand autocalibration
- **Front-panel system I/O access**
- 16-Bit bidirectional TTL digital I/O port
- Conforms to PCI Express Specification revision 1.0a; x1 link operating at 2.5Gbps
- **3U VPX form factor**

Typical Applications

- ✓ High Performance Data Acquisition
- ✓ Arbitrary Waveform Generation
- ✓ Event Capture
- ✓ Ultrasound
- ✓ Robotics
- ✓ Positioning Systems

--- PRELIMINARY ---

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Functional Description

The 16-Bit CCVPX-16AISS8AO4C analog I/O module samples and digitizes eight input channels simultaneously at rates up to 2.0 Megasamples per second for each channel. The resulting 16-bit sampled data is available to the PCI Express host through a 256K-Sample FIFO buffer. Sampling can be controlled in groups of 1 through 8 channels, and the sample clock can be generated from an internal rate generator, or through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are software-selectable as ±10V, ±5V, or ±2.5V. The inputs can be divided into two channel groups with independent range assignments.

Four analog output channels provide software-selected output ranges of ±10V, ±5V or ±2.5V independently of the input range selection, and are accessed either directly through dedicated control registers, or output data can be routed through a 256K-Sample FIFO buffer for waveform generation. Output clocking rates are supported up to 1.0 Megasamples per second. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

On-demand autocalibration determines and applies offset and gain correction values for all input and output channels. A selftest input switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host..

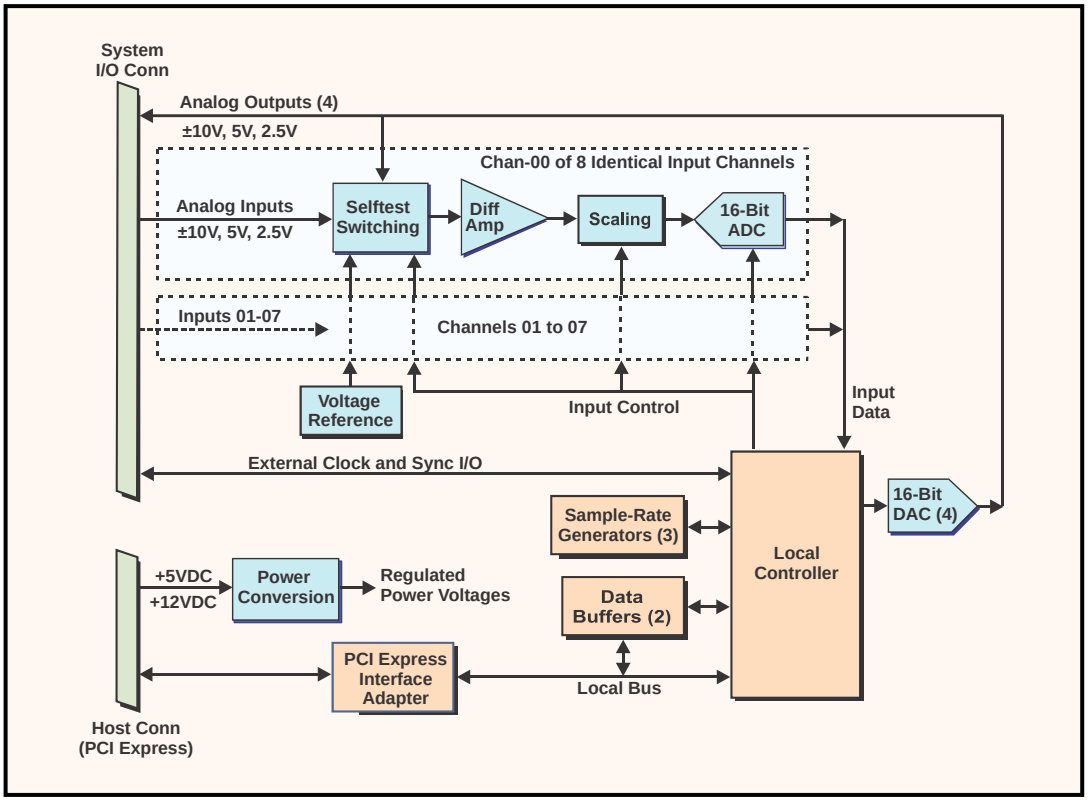

Figure 1. CCVPX-16AISS8AO4C; Functional Organization

This product conforms to the VPX baseline standard ANSI/VITA 46.0-2007 (R2013). System connections are made at the front panel through a high-density front-panel I/O connector. Power requirements consist of +12VDC and +5VDC in compliance with the VPX specification, and operation over the specified temperature range is achieved with standard conduction cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions.

Analog Input Characteristics:

Configuration:	Eight differential analog input channels; Dedicated 16-Bit ADC per channel. Optional 4-Channel version available.
Voltage Ranges:	Independently assignable between two groups of input channels as: ±10V, ±5V or ±2.5V full scale.
Input Impedance:	2 Megohms Line-Line in parallel with 40pF.
Bias Current:	100 nanoamps typical all ranges
Crosstalk Rejection:	84dB, DC-10kHz. 70dB at 100kHz.
Signal/Noise Ratio (SNR):	82dB typical; 10Hz to 500kHz
Common Mode Rejection:	65dB DC-10kHz; 53dB at 100kHz. Typical with CMV = ±10V, Vin = Zero.
Overvoltage Protection:	±25V with power applied, ±15 Volts with power removed.

Analog Input Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Sample Rate:	Zero to 2.0 MSPS per channel		
Sampling Mode::	Simultaneous; all active input channels		
DC Accuracy:	Range	Midscale Accuracy	Fullscale Accuracy
(Maximum composite error after autocalibration)	±10V	± 2mV	± 5mV
	±5V	± 1mV	± 3mV
	±2.5V	± 0.8mV	± 2mV
Small Signal Bandwidth:	Zero to 5MHz, -3dB, all ranges		
Settling Time:	500ns to 0.1%; halfscale step; typical; all ranges.		
Power Bandwidth:	3MHz, 10Vp-p, -3dB		
Integral Nonlinearity:	±0.007 percent FSR (FSR = fullscale range; e.g.: 20Von ±10Vrange).		
Differential Nonlinearity:	±0.003 percent FSR.		

Analog Input Operating Modes and Controls

Input Data Buffer:	**256K-sample FIFO**
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generators:	Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 4-2,000,000 sample clocks per second, using 24-Bit dividers from the 64MHz master clock frequency.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.
Principal Status Register:	Consolidates critical status flags at a single Longword location.
Input Data Format:	16 Bits. Selectable as offset binary or two's complement. First-channel and end of-burst tagged.

Analog Output Characteristics:

Configuration:	Four single-ended output channels. (Two external and two internal output channels if the SMA inputs I/O ordering option is specified).
Voltage Ranges:	±10, ±5 or ±2.5 Volts; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum at I/O connector pins.
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to ±3ma per channel
Load Capacitance:	Stable with any load capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	7 nV-s, typical on ±5V range

Analog Output Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Output Access:	Direct register access or 256K-Sample FIFO buffer.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±4mV	±8mV
	±5V	±2mV	±6mV
	±2.5V	±1.5mV	±4mV
Settling Time:	2us to 0.1 percent, typical with halfscale step, no-load.		
Crosstalk Rejection:	70 dB minimum, DC-100 kHz		
Integral Nonlinearity:	±0.007 percent of FSR, maximum		
Differential Nonlinearity:	±0.002 percent of FSR, maximum		
Output Data Format:	16 Bits. Same format as selected for analog inputs.		

Analog Output Operating Modes and Controls

Output Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock.
Burst Triggering Sources:	TTL external Trigger I/O (shared with analog inputs), Software trigger.
Clocking Modes:	Continuous or periodic clocking, and triggered burst.
Internal Rate Generator:	Programmable from 4-1,000,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Clock I/O:	TTL, bidirectional. Zero to 1,000,000 sample clocks per second.
Output Data Format:	16-Bits. Selectable as offset binary or two's complement.

Digital I/O Port:

Dual Independent 8-Bit bidirectional I/O ports. Standard TTL levels. Direct register Access.
±8 mA loading when configured as outputs. 0.15 mA source when configured as inputs.

Host Bus Compatibility:

Conforms to VPX VITA 46.0.
Also conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps.
DMA transfers as bus master with two DMA channels.

Power Requirements

+5VDC ±0.2 VDC, 0.8Amps typical, 1.0 Amps maximum.
+12VDC ±0.4 VDC, 0.3 Amps typical, 0.4 Amps maximum
Total power consumption: 7.6 Watts typical, 10 Watts maximum. (Outputs fully loaded).

Mechanical Characteristics

Height: 18.8mm (0.74 in)
Depth: 170.6 mm (6.717 in)
Width: 100.0 mm (3.937 in)
Shield: Side-1 is protected by an EMI shield.
Thermal transfer rails are provided for conduction cooling.

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +80 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating and Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Standard conduction cooling thermal interfaces.

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number **CCVPX-16AISS8AO4C-8-4 -64.000M-0** describes a 3U VPX module with eight input channels, four output channels, a standard 64MHz master clock frequency, and no custom features.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	8 Input Channels	A = 8
	4 Input Channels	A = 4
Number of Output Channels	4 Output Channels	B = 4
	No Analog Outputs	B = 0
Master Clock Frequency	64.000MHz	C = 64.000M
	Custom frequency; 64-66 MHz	C = (Custom frequency)M
Custom Feature	---	D *

* Blank or zero (0) if no custom feature applies.

System Interface Connector

Table 1. System I/O Connector Pin Functions

Pin	Signal	Pin	Signal
43	OUTPUT RTN	---	---
42	OUTPUT RTN	85	ANA OUT 00
41	OUTPUT RTN	84	ANA OUT 01
40	OUTPUT RTN	83	ANA OUT 02
39	OUTPUT RTN	82	ANA OUT 03
38	INPUT RTN	81	INPUT RTN
37	INP00_LO [1]	80	INP00_HI [1]
36	INPUT RTN	79	INPUT RTN
35	INP01_LO [1]	78	INP01_HI [1]
34	INPUT RTN	77	INPUT RTN
33	INP02_LO [2]	76	INP02_HI [2]
32	INPUT RTN	75	INPUT RTN
31	INP03_LO [2]	74	INP03_HI [2]
30	INPUT RTN	73	INPUT RTN
29	INP04_LO [1]	72	INP04_HI [1]
28	INPUT RTN	71	INPUT RTN
27	INP05_LO [1]	70	INP05_HI [1]
26	INPUT RTN	69	INPUT RTN
25	INP06_LO [2]	68	INP06_HI [2]
24	INPUT RTN	67	INPUT RTN
23	INP07_LO [2]	66	INP07_HI [2]
22	INPUT RTN	65	INPUT RTN
21	VTEST RTN	64	VTEST
20	INPUT RTN	63	INPUT RTN
19	DIGITAL RTN	62	DIO 00
18	DIGITAL RTN	61	DIO 01
17	DIGITAL RTN	60	DIO 02
16	DIGITAL RTN	59	DIO 03
15	DIGITAL RTN	58	DIO 04
14	DIGITAL RTN	57	DIO 05
13	DIGITAL RTN	56	DIO 06
12	DIGITAL RTN	55	DIO 07
11	DIGITAL RTN	54	DIO 08
10	DIGITAL RTN	53	DIO 09
9	DIGITAL RTN	52	DIO 10
8	DIGITAL RTN	51	DIO 11
7	DIGITAL RTN	50	DIO 12
6	DIGITAL RTN	49	DIO 13
5	DIGITAL RTN	48	DIO 14
4	DIGITAL RTN	47	DIO 15
3	DIGITAL RTN	46	OUTPUT CLK I/O
2	DIGITAL RTN	45	INPUT CLK I/O
1	DIGITAL RTN	44	TRIGGER I/O

[1] Input Group-A.
[2] Input Group-B.
(4 input-channel modules contain input Channels 00-03).

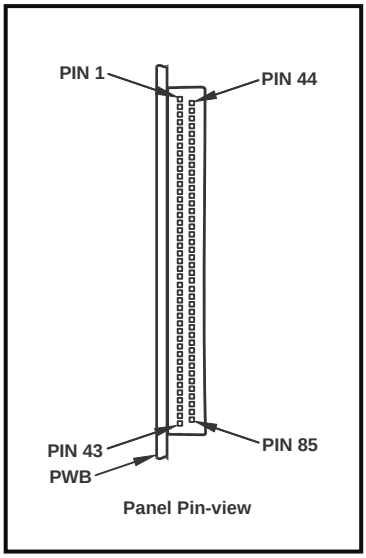

Figure 2. System I/O Connector

System I/O Mating Connector:
Omnetics # MNPO-85-DD-N-EJS-C, dual-row, straight tail.
(Assembled cables available)