DAC-Q30

Quad 12.0 Gsps 16-bit DAC FMC+ Module. VITA 57.4

The DAC-Q30 FMC+ module from DEG is a high sample rate, 16 bit quad channel DAC module. The Analog Devices AD9174 DAC device operates at 3.0 Gsps natively and up to 12.0 Gsps in interpolation mode. A VITA 57.4-compliant FPGA Mezzanine Card (FMC+) interface, the DAC-Q30 offers industry wide platform compatibility with the PCIe/VME/VXS/VPX carrier board of your choice. The DAC-Q30 and associated HDL firmware are compatible with Xilinx® FPGAs.

BENEFITS

- Quad Channel DAC on a Single FMC+ Module
- Wide Dynamic Range
- Convection and Conduction-Cooled Versions
- Enables SWaP-C Sensitive Systems: High Density, Small Footprint, Low Power

FEATURES

- Quad Channel 3.0 Gsps 16-bit DAC : 12 Gsps in Interpolation Mode
- JESD204B SERDES Interface: x 16 Lanes DAC @ 15.0 Gbs per Lane
- Built-in Clock Jitter Cleaner
- Multiple Configurable Data Channel Interpolation Options

DAC PERFORMANCE

- SFDR = f_{OUT} = 500 MHz−76 dBc @ 3.0 Gsps
- SFDR = f_{OUT} = 1850 MHz−80 dBc @ 12.0 Gsps
- NSD = f_{OUT} = 500 MHz−163 dBm/Hz @ 3.0 Gsps
- NSD = f_{OUT} = 2150 MHz−164 dBm/Hz @ 12.0 Gsps

Flexible, cost-effective solution

By coupling this core architecture with the compact and flexible VITA 57.4 form factor, DEG has enabled customers to rapidly and cost-effectively build compact systems with significant SWaP-C benefits. By packing four high-performance DAC channels on a single FMC+ module, DEG is enabling a new generation of radar, jammer and high-performance communication applications.

Performance

The DAC-Q30 incorporates the JESD204B SERDES Interface standard. The DAC-Q30 utilizes 16 JESD204B lanes from the carrier board FPGA. Sustained data transfer rates of up to 15.0 Gbytes/sec. are supported.

The DEG Advantage

DEG has developed a broad ecosystem of tightly integrated ADC, DAC and FPGA carrier products to suit a wide range of defense applications. DEG is committed to delivering industry leading , embedded computing functionality and performance; the DAC-Q30 continues this tradition.

Delphi Engineering is a AS9100D certified company

Clocks

The DAC-Q30 provides an onboard synthesizer which covers the entire DAC sampling range. Delphi incorporates a clock jitter cleaner on the DAC-Q30, which improves DAC performance.

The following sources can be selected for the synthesizer:

• External reference signal

• Low noise onboard reference – 20 ppm accuracy over the entire temperature range of the product

Trigger

A trigger event is initiated by a positive transition. The trigger threshold is software-controllable over a wide range on the trigger input. An auto-trigger feature enables continuous signal capture or synthesis without a trigger.

DACLink

Delphi's DACLink VHDL source code provides the specific DAC interface and control logic necessary to integrate with your carrier board FPGA.

DACLink capabilities include: onboard/external reference clock control, trigger threshold control, and full control over DAC devices.

DAC-Q30 Performance Specification

DAC Specifications	
Number of DAC channels	4
Sampling rate	3.0 Gsps
Sampling rate w/ Interpolation	12.0 Gsps
Output bandwidth	6.0 GHz
Output impedance	50 Ω, AC-coupled
Clock and Trigger Specifications	
Ext. Reference Clock Input	10 MHz to 750 MHz
Trigger input	Single-ended 50 Ω

DAC-Q30 Environmentals

Environmental Specifications	Commercial	Conduction-Cooled
Operating temperature	0°C to +50°C	-40°C to +85°C (at card edge)
Storage temperature	-55°C to +85°C	-55°C to +125°C
Humidity (non-condensing)	0 to 95%	0 to 100%

About DEG

The Delphi Engineering Group (DEG) provides a full range of high-performance COTS-based and customized digital receiver technology, products, and services for mission-critical applications in the aerospace, defense, and communications industries.

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