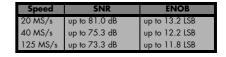


# DN6.59x - 48 channel 16 bit digitizerNETBOX up to 125 MS/s

- 24, 32, 40 or 48 channels with 20 MS/s up to 125 MS/s
- Software selectable single-ended or differential inputs
- Simultaneously sampling on all channels
- Separate ADC and amplifier per channel
- complete on-board calibration
- 6 input ranges: ±200 mV up to ±10 V
- 64 MSample/channel standard acquisition memory
- Programmable input offset of ±100%
- Window, pulse width, re-arm, spike, OR/AND trigger
- Streaming, ABA mode, Multiple Recording, Gated Sampling, Timestamps





- Ethernet Remote Instrument
- LXI Core 2011 compatible
- GBit Ethernet Interface
- Sustained streaming mode up to 70 MB/s
- Direct Connection to PC/Laptop
- Connect anywhere in company LAN
- Embedded Webserver for Maintenance/Updates
- Embedded Server option for open Linux platform

Operating Systems	SBench 6 Professional Included	<u>Drivers</u>
• Windows 7 (SP1), 8, 10,	• Acquisition, Generation and Display of analog and	<ul> <li>LabVIEW, MATLAB, LabWindows/CVI</li> </ul>
Server 2008 R2 and newer	digital data	<ul> <li>Visual C++, C++ Builder, GNU C++,</li> </ul>
• Linux Kernel 2.6, 3.x, 4.x, 5.x	Calculation, FFT	VB.NET, C#, J#, Delphi, Java, Python
• Windows/Linux 32 and 64 bit	<ul> <li>Documentation and Import, Export</li> </ul>	• IVI

Model	Single-Ende	d Inputs	Differential Inputs				
DN6.592-24	24 channels	20 MS/s	12 channels	20 MS/s			
DN6.592-32	32 channels	20 MS/s	16 channels	20 MS/s			
DN6.592-40	40 channels	20 MS/s	20 channels	20 MS/s			
DN6.592-48	48 channels	20 MS/s	24 channels	20 MS/s			
DN6.593-24	24 channels	40 MS/s	12 channels	40 MS/s			
DN6.593-32	32 channels	40 MS/s	16 channels	40 MS/s			
DN6.593-40	40 channels	40 MS/s	20 channels	40 MS/s			
DN6.593-48	48 channels	40 MS/s	24 channels	40 MS/s			
DN6.596-24	12 channels 24 channels	125 MS/s 80 MS/s	12 channels	125 MS/s			
DN6.596-32	16 channels 32 channels	125 MS/s 80 MS/s	16 channels	125 MS/s			
DN6.596-40	20 channels 40 channels	125 MS/s 80 MS/s	20 channels	125 MS/s			
DN6.596-48	24 channels 48 channels	125 MS/s 80 MS/s	24 channels	125 MS/s			

# **General Information**

The digitizerNETBOX DN6.59x series allows recording of up to 48 channels with sampling rates of 80 MS/s or 24 channels with sampling rates of 125 MS/s. These Ethernet Remote instruments offer outstanding A/D features both in resolution and signal quality. The inputs can be switched between Single-Ended with a programmable offset and True Differential. If used in differential mode each two inputs are connected together reducing the number of available channels by half.

Importantly, the high-resolution 16-bit ADCs deliver sixteen times more resolution than digitizers using older 12-bit technology and 256 times more resolution than what is available from digital scopes that commonly use 8-bit ADCs. The digitizerNETBOX can be installed anywhere in the company LAN and can be remotely controlled from a host PC.

# Software Support

### Windows Support

The digitizerNETBOX/generatorNETBOX can be accessed from Windows 7, Windows 8, Windows 10 (each 32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, LabWindows/CVI, Delphi, Visual Basic, VB.NET, C#, J#, Python, Java and IVI are included.

### Linux Support



The digitizerNETBOX/generatorNETBOX can be accessed from any Linux system. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++, Python as well as drivers for

MATLAB for Linux. SBench 6, the powerful data acquisition and analysis software from Spectrum is also included as a Linux version.

### **Discovery Protocol**

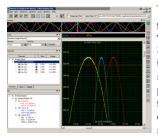
Physical Location	
Bus No	0
Device No	0
Function No	0
Slot No	0
IP	192.168.169.14
VISA	TCPIP[0]::192.168.169.14::inst0::INSTR

The Discovery function helps you to find and identify any Spectrum LXI instruments, like the digitizerNETBOX and generatorNETBOX, avail-

able to your computer on the network. The Discovery function will also locate any Spectrum card products that are managed by an installed Spectrum Remote Server somewhere on the network.

After running the discovery function the card information is cached and can be directly accessed by SBench 6. Furthermore the qualified VISA address is returned and can be used by any software to access the remote instrument.

## SBench 6 Professional



The digitizerNETBOX and generatorNETBOX can be used with Spectrum's powerful software SBench 6 – a Professional license for the software is already installed in the box. SBench 6 supports all of the standard features of the instrument. It has a variety of display windows as well as analysis, export and documentation

functions.

- Available for Windows XP, Vista, Windows 7, Windows 8, Windows 10 and Linux
- Easy to use interface with drag and drop, docking windows and context menus
- Display of analog and digital data, X-Y display, frequency domain and spread signals
- Designed to handle several GBytes of data
- Fast data preview functions

### IVI Driver

The IVI standards define an open driver architecture, a set of instrument classes, and shared software components. Together these provide critical elements needed for instrument interchangeability. IVI's defined Application Programming Interfaces (APIs) standardize common measurement functions reducing the time needed to learn a new IVI instrument.

The Spectrum products to be accessed with the IVI driver can be locally installed data acquisition cards, remotely installed data acquisition cards or remote LXI instruments like

digitizerNETBOX/generatorNETBOX. To maximize the compatibility with existing IVI based software installations, the Spectrum IVI

driver supports IVI Scope, IVI Digitizer and IVI FGen class with IVI-C and IVI-COM interfaces.

### **Third-party Software Products**

Most popular third-party software products, such as LabVIEW, MATLAB or LabWindows/CVI are supported. All drivers come with examples and detailed documentation.

## Embedded Webserver



The integrated webserver follows the LXI standard and gathers information on the product, set up of the Ethernet configuration and current status. It also allows the setting of a configuration password, access to documentation and updating of the complete instrument firmware, including the embedded remote server and the webserver.

### Hardware features and options

3.32.13608

-TCPIP::192.168.169.20::INSTR

#### **LXI Instrument**



The digitizerNETBOX and generatorNETBOX are fully LXI instrument compatible to LXI Core 2011 following the LXI Device Specification

2011 rev. 1.4. The digitizerNETBOX/generatorNETBOX has been tested and approved by the LXI Consortium.

Located on the front panel is the main on/off switch, LEDs showing the LXI and Acquisition status and the LAN reset switch.

#### Front Panel



Standard BNC connectors are used for all analog input or output signals and all trigger and clock signals. No special adapter cables are needed and the connection is secure even when used in a moving environment.

Custom front panels are available es, be it SMA, LEMO connectors or

on request even for small series, be it SMA,  $\dot{\text{LEMO}}$  connectors or custom specific connectors.

#### Ethernet Connectivity



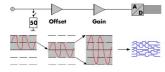
The GBit Ethernet connection can be used with standard COTS Ethernet cabling. The integration into a standard LAN allows to connect the digitizerNETBOX/generatorNET-BOX either directly to a desktop PC or Laptop or it is possible to place the instrument somewhere in the

company LAN and access it from any desktop over the LAN.

#### **Boot on Power on Option**

The digitizerNETBOX/generatorNETBOX can be factory configured to automatically start and boot upon availability of the input power rail. That way the instrument will automatically become available again upon loss of input power.

### Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed

between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

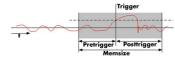
#### **Differential inputs**

With a simple software command the inputs can individually be switched from single-ended (in relation to ground) to differential by combining each two single-ended inputs to one differential input. When the inputs are used in differential mode the A/D converter measures the difference between two lines with relation to system ground.

#### Automatic on-board calibration

All of the channels are calibrated in factory before the board is shipped. To compensate for different variations like PC power supply, temperature and aging, the software driver provides routines for an automatic onboard offset and gain calibration of all input ranges. All the cards contain a high precision on-board calibration reference.

#### **Ring buffer mode**



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a

trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

#### FIFO mode

The FIFO mode is designed for continuous data transfer between remote instrument and PC memory or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

#### **Channel trigger**

The data acquisition instruments offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

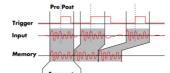
#### External trigger I/O

All instruments can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

#### Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

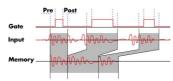
### Multiple Recording



The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in be-

tween. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

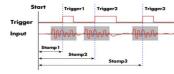
#### Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start

of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

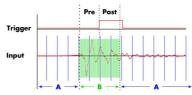
#### **Timestamp**



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, ex-

ternally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

#### ABA mode



The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact

position of the trigger events is stored as timestamps in an extra memory.

#### **Option Embedded Server**



The option turns the digitizer-NETBOX/generatorNETBOX in a powerful PC that allows to run own programs on a small and remote data acquisition system. The digitizerNET-BOX/generatorNETBOX is en-

hanced by more memory, a powerful CPU, a freely accessable internal SSD and a remote software development access method.

The digitizerNETBOX/generatorNETBOX can either run connected to LAN or it can run totally independent, storing data to the internal SSD. The original digitizerNETBOX/generatorNETBOX remote instrument functionality is still 100% available. Running the embedded server option it is possible to pre-calculate results based on the acquired data, store acquisitions locally and to transfer just the required data or results parts in a client-server based software structure. A different example for the

digitizerNETBOX/generatorNETBOX embedded server is surveillance/logger application which can run totally independent for days and send notification emails only over LAN or offloads stored data as soon as it's connected again.

Access to the embedded server is done through a standard text based Linux shell based on the ssh secure shell.

#### External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

#### **Reference clock**



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality

measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

# DN2 / DN6 Technical Data

## Analog Inputs

Resolution		16 bit (can be reduced to acquire sim	nultaneous digital inputs)
Input Range	software programmable	±200 mV, ±500 mV, ±1 V, ±2 V, ±5	
Input Type	software programmable	Single-ended or True Differential	V, ±10 V
Input Offset (single-ended)	software programmable	programmable to $\pm 100\%$ of input rar	and in stone of 1%
ADC Differential non linearity (DNL)	ADC only	592x: ±0.2/±0.8 LSB (typ./max.) 593x: ±0.5/±0.9 LSB (typ./max.) 594x: ±0.5/±0.9 LSB (typ./max.)	ige in sieps of 176
ADC Integral non linearity (INL)	ADC only	592x: ±1.0/±2.3 LSB (typ./max.) 593x: ±2.0/±7.5 LSB (typ./max.) 594x: ±2.0/±7.5 LSB (typ./max.) 596x: ±2.0/±7.5 LSB (typ./max.)	
Offset error (full speed), DC signal	after warm-up and calibration	≤ 0.1% of range	
Gain error (full speed), DC signal	after warm-up and calibration	≤ 0.1% of reading	
AC accuracy	1 kHz signal	$\leq 0.3\%$ of reading	
AC accuracy	50 kHz signal	≤ 0.5% of reading	
Crosstalk: Signal 1 MHz, 50 $\Omega$	$\begin{array}{l} \text{range} \leq \pm 1 V \\ \text{range} \geq \pm 2 V \end{array}$	≤ 95 dB on adjacent channels ≤ 90 dB on adjacent channels	
Crosstalk: Signal 10 MHz, 50 $\Omega$	$\begin{array}{l} \text{range} \leq \pm 1 V \\ \text{range} \geq \pm 2 V \end{array}$	≤ 87 dB on adjacent channels ≤ 85 dB on adjacent channels	
Analog Input impedance	software programmable	50 Ω /1 MΩ    30 pF	
Analog input coupling	fixed	DC	
Over voltage protection	range ≤ ±1V	±5 V (1 MΩ), 3.5 Vrms (50 Ω)	
Over voltage protection	range ≥ ±2V	±50 V (1 MΩ), 5 Vrms (50 Ω)	
CMRR (Common Mode Rejection Ratio)	range ≤ ±1V	100 kHz: 75 dB, 1 MHz: 60 dB, 10	MHz: 40 dB
CMRR (Common Mode Rejection Ratio)	range ≥ ±2V	100 kHz: 55 dB, 1 MHz: 52 dB, 10	MHz: 50 dB
Channel selection (single-ended inputs)	software programmable	1, 2, 4 or 8 channels (maximum is m	odel dependent)
Channel selection (true differential inputs)	software programmable	1, 2 or 4 channels (maximum is mode	el dependent)
<b>Frigger</b> Available trigger modes Trigger level resolution	software programmable software programmable	Channel Trigger, External, Software, V 14 bit	Window, Pulse, Re-Arm, Spike, Or/And, Delay
ingger level resolution	sonware programmable		
Trigger edge	software programmable	Rising edge, falling edge or both edg	es
Trigger pulse width	software programmable	0 to [4G - 1] samples in steps of 1 sa	mple
Trigger delay	software programmable	0 to [4G - 1] samples in steps of 1 sa	mples
Trigger holdoff (for Multi, ABA, Gate)	software programmable	0 to [4G - 1] samples in steps of 1 sa	mples
Multi, ABA, Gate: re-arming time		< 24 samples (+ programmed pretrig	ger + programmed holdoff )
Pretrigger at Multi, ABA, Gate, FIFO	software programmable	8 up to [32 kSamples / number of ac	tive channels] in steps of 8
Posttrigger	software programmable	8 up to [8G - 4] samples in steps of 8	(defining pretrigger in standard scope mode)
Memory depth	software programmable	8 up to [installed memory / number of	of active channels] samples in steps of 8
Multiple Recording/ABA segment size			a delive chamileis] samples in sieps of o
	software programmable	8 up to [installed memory / number c	of active channels] samples in steps of 8
Internal/External trigger accuracy	software programmable	8 up to [installed memory / number of 1 sample	
Timestamp modes	software programmable software programmable	1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, RefClock: 24 bit upper co	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock)
		1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, RefClock: 24 bit upper co 40 bit lower co	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock)
Timestamp modes Data format Extra data	software programmable	1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, RefClock: 24 bit upper co 40 bit lower co	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock) unter (increments with sample clock, reset with RefClock)
Timestamp modes Data format Extra data Size per stamp External trigger	software programmable	1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, i RefClock: 24 bit upper co 40 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes Ext	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock) unter (increments with sample clock, reset with RefClock) is at trigger time, trigger source (for OR trigger) X1, X2, X3
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type	software programmable	1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, i RefClock: 24 bit upper co 40 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes <b>Ext</b> Single level comparator	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock is at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger impedance	software programmable	1 sample         Standard, Startreset, external reference         Std., Startreset:       64 bit counter, it         RefClock:       24 bit upper co         40 bit lower co         none, acquisition of X1/X2/X3 inputs         128 bit = 16 bytes         Ext         Single level comparator         50 Ω / 5 kΩ	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock s at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs For electrical specifications refer to
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger impedance	software programmable	1 sample Standard, Startreset, external reference Std., Startreset: 64 bit counter, i RefClock: 24 bit upper co 40 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes <b>Ext</b> Single level comparator	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock is at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger impedance External trigger input level	software programmable	1 sample         Standard, Startreset, external reference         Std., Startreset:       64 bit counter, it         RefClock:       24 bit upper co         40 bit lower co         none, acquisition of X1/X2/X3 inputs         128 bit = 16 bytes         Ext         Single level comparator         50 Ω / 5 kΩ	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock s at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs For electrical specifications refer to
Extra data Size per stamp External trigger External trigger type	software programmable	$\begin{array}{llllllllllllllllllllllllllllllllllll$	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock s at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs For electrical specifications refer to
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger impedance External trigger over voltage protection External trigger over voltage protection External trigger sensitivity	software programmable	1 sample Standard, Startreset, external references Std., Startreset: 64 bit counter, i RefClock: 24 bit upper co 40 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes <b>Ext</b> Single level comparator 50 $\Omega$ / 5 k $\Omega$ ±5 V (5 k $\Omega$ ), ±2.5 V (50 $\Omega$ ), ±20 V (5 k $\Omega$ ), 5 Vrms (50 $\Omega$ )	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start unter (increment with RefClock) unter (increments with sample clock, reset with RefClock s at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs For electrical specifications refer to
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger impedance External trigger input level External trigger over voltage protection External trigger sensitivity (minimum required signal swing)	software programmable software programmable software programmable software programmable 50 Ω	1 sample Standard, Startreset, external references Std., Startreset: 64 bit counter, if RefClock: 24 bit upper co 40 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes <b>Ext</b> Single level comparator 50 $\Omega$ / 5 k $\Omega$ ±5 V (5 k $\Omega$ ), ±2.5 V (50 $\Omega$ ), ±20 V (5 k $\Omega$ ), 5 Vrms (50 $\Omega$ ) 200 mVpp ±5 V in steps of 1 mV DC to 400 MHz	of active channels] samples in steps of 8 the clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock) unter (increments with sample clock, reset with RefClock) is at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V IVTTL logic inputs For electrical specifications refer to "Multi Purpose I/O lines" section.
Timestamp modes Data format Extra data Size per stamp External trigger External trigger type External trigger input level External trigger over voltage protection External trigger sensitivity (minimum required signal swing) External trigger level	software programmable software programmable software programmable	1 sample Standard, Startreset, external references Std., Startreset: 64 bit counter, i RefClock: 24 bit upper co A0 bit lower co none, acquisition of X1/X2/X3 inputs 128 bit = 16 bytes <b>Ext</b> Single level comparator $50 \Omega / 5 k\Omega$ $\pm 5 V (5 k\Omega), \pm 2.5 V (50 \Omega),$ $\pm 20 V (5 k\Omega), 5 Vrms (50 \Omega)$ 200 mVpp $\pm 5 V$ in steps of 1 mV	of active channels] samples in steps of 8 ce clock on X1 (e.g. PPS from GPS, IRIG-B) increments with sample clock (reset manually or on start) unter (increment with RefClock) unter (increments with sample clock, reset with RefClock) is at trigger time, trigger source (for OR trigger) <b>X1, X2, X3</b> 3.3V LVTTL logic inputs For electrical specifications refer to "Multi Purpose I/O lines" section.

### <u>Clock</u>

Clock Modes	software programmable	internal PLL, external clock, external reference clock, sync
Internal clock range (PLL mode)	software programmable	see "Clock Limitations and Bandwidth" table below
Internal clock accuracy		$\leq \pm 1.0$ ppm (at time of calibration in production)
Internal clock aging		≤ ±0.5 ppm / year
PLL clock setup granularity (int. or ext. reference)		1 Hz
External reference clock range	software programmable	128 kHz up to 125 MHz
Direct external clock to internal clock delay		4.3 ns
Direct external clock range		see "Clock Limitations and Bandwidth" table below
External clock type		Single level comparator
External clock input level		±5 V (5 kΩ), ±2.5 V (50 Ω),
External clock input impedance	software programmable	50 Ω / 5 kΩ
External clock over voltage protection		±20 V (5 kΩ), 5 Vrms (50 Ω)
External clock sensitivity (minimum required signal swing)		200 мVpp
External clock level	software programmable	±5 V in steps of 1mV
External clock edge		rising edge used
External reference clock input duty cycle		45% - 55%
Clock output electrical specification		Available via Multi Purpose output X0. Refer to "Multi Purpose I/O lines" section.
Synchronization clock multiplier "N" for different clocks on synchronized cards	software programmable	N being a multiplier (1, 2, 3, 4, 5, Max) of the card with the currently slowest sampling clock. The card maximum (see "Clock Limitations and Bandwidth" table below) must not be exceeded.
ABA mode clock divider for slow clock	software programmable	8 up to (64k - 8) in steps of 8
Channel to channel skew on one card		< 200 ps (typical)
Skew between star-hub synchronized cards		TBD

#### **Connectors**

Analog Inputs		9 mm BNC female (one for each single-ended input)	Cable-Type: Cab-9m-xx-xx
Trigger Input		9 mm BNC female	Cable-Type: Cab-9m-xx-xx
Clock/Reference Clock Input		9 mm BNC female	Cable-Type: Cab-9m-xx-xx
Clock Output, Multi-Purpose X0		9 mm BNC female	Cable-Type: Cab-9m-xx-xx
Multi-Purpose I/O X1, X2, X3	Programmable Direction	9 mm BNC female	Cable-Type: Cab-9m-xx-xx

## Option digitizerNETBOX/generatorNETBOX embedded server (DN2.xxx-Emb, DN6.xxx-Emb)

CPU System memory System data storage Development access Accessible Hardware Integrated operating system

#### **Ethernet specific details**

LAN Connection LAN Speed Sustained Streaming speed

Used LAN Ports

#### **Power connection details**

Mains AC power supply AC power supply connector Power supply cord

### Certification, Compliance, Warranty

EMC Immunity EMC Emission Product warranty Software and firmware updates Intel Quad Core 2 GHz 4 GByte RAM Internal 128 GByte SSD Remote Linux command shell (ssh), no graphical interface (GUI) available Full access to Spectrum instruments, LAN, front panel LEDs, RAM, SSD OpenSuse 12.2 with kernel 4.4.7.

 Standard RI45

 Auto Sensing: GBit Ethernet, 100BASE-T, 10BASE-T

 DN2.20, DN2.46, DN2.47, DN2.49, DN2.60
 up to 70 MByte/s

 DN6.46, DN6.49
 up to 100 MByte/s

 DN2.59, DN2.22, DN2.44, DN2.66
 up to 100 MByte/s

 DN6.59, DN6.22, DN6.44, DN6.66
 mDNS Daemon: 5353

 VISA Discovery Protocol: 111, 9757
 UPNP Daemon: 1900

Input voltage: 100 to 240 VAC, 50 to 60 Hz IEC 60320-1-C14 (PC standard coupler) power cord included for Schuko contact (CEE 7/7)

Compliant with CE Mark Compliant with CE Mark 5 years starting with the day of delivery Life-time, free of charge

# **Clock Limitations and Bandwidth**

	M2p.592x, DN2.592-xx DN6.592-xx	M2p.593x DN2.593-xx DN6.593-xx	M2p.594x	M2p.596x DN2.596-xx DN6.596-xx
max internal clock (non-synchronized cards)	20 MS/s	40 MS/s	80 MS/s	125 MS/s
min internal clock (non-synchronized cards)	1 kS/s	1 kS/s	1 kS/s	1 kS/s
max internal clock (cards synchronized via star-hub)	20 MS/s	40 MS/s	80 MS/s	125 MS/s
min internal clock (cards synchronized via star-hub)	128 kS/s	128 kS/s	128 kS/s	128 kS/s
max direct external clock	20 MS/s	40 MS/s	80 MS/s	125 MS/s
min direct external clock	1 MS/s	1 MS/s	1 MS/s	1 MS/s
-3 dB analog input bandwidth	> 10 MHz	> 20 MHz	> 40 MHz	> 60 MHz

# RMS Noise Level (Zero Noise), typical figures

	11	M2p.592x, DN2.592-xx, DN6.592-xx										
Input Range	±200	±200 mV		±500 mV		±l		±2 V		±5 V		0 V 0
Voltage resolution	6.1	μV	15.3 μV		30.5 μV		61.0 μV		152.6 μV		305.2 μV	
50 Ω	<4.0 LSB	<25 μV	<2.6 LSB	<40 μV	<2.1 LSB	<65 μV	<4.3 LSB	<263 μV	<2.6 LSB	<397 μV	<2.1 LSB	<641 μV
1 MΩ	<4.5 LSB	<28 µV	<3.0 LSB	<46 μV	<2.5 LSB	<107 μV	<4.5 LSB	<275 μV	<3.0 LSB	<458 μV	<2.5 LSB	<763 μV
1 ΜΩ	<4.5 LSB	<28 µV	<3.0 LSB	<46 μV	<2.5 LSB	<107 µV	<4.5 LSB	<275 μV	<3.0 LSB	<458	μV	μV <2.5 LSB

	M2p.593x, DN2.593-xx, DN6.593-xx											
Input Range	±200 mV		±500 mV		±l		±2 V		±5 V		±10 V	
Voltage resolution	6.1 μV		15.3 μV		30.5 μV		61.0 μV		152.6 μV		305.2 μV	
50 Ω	<6.0 LSB	<37 μV	<5.0 LSB	<77 μV	<4.5 LSB	<138 µV	<6.5 LSB	<397 μV	<5.0 LSB	<763 μV	<4.5 LSB	<1.4 mV
1 ΜΩ	<6.5 LSB	<40 µV	<5.0 LSB	<77 μV	<4.5 LSB	<138 µV	<6.5 LSB	<397 μV	<5.0 LSB	<763 μV	<4.5 LSB	<1.4 mV

	M2p.594x											
put Range	±200 m\	V ±	±500 mV		±l		±2 V		±5 V		0 V 0	
oltage resolution	6.1 μV		15.3 μV		30.5 μV		61.0 µV		152.6 μV		305.2 μV	
0 Ω	<7.0 LSB <43	3 μV <5.5 LS	iB <85μV	<4.5 LSB	<138 µV	<7.5 LSB	<458 µV	<5.5 LSB	<840 µV	<4.5 LSB	<1.4 mV	
MΩ	<7.5 LSB <40	6 µV <5.8 LS	iB <89 μV	<4.5 LSB	<138 µV	<7.7 LSB	<470 µV	<5.8 LSB	<886 µV	<4.5 LSB	<1.4 mV	
MΩ	<7.5 LSB <40	6 µV <5.8 LS	-89 μV	<4.5 LSB	<138 µV	<7.7 LSB	<470 μV	<5.8 LSB	<886 µV	<4.5 LSB		

	M2p.596x, DN2.596-xx, DN6.596-xx										
Input Range	±200 mV		±500 mV		±l		±2 V		±5 V		0 V 0
Voltage resolution	6.1 μV 15.3 μV		30.5 μV		61.0 μV		152.6 μV		305.2 μV		
50 Ω	<9.0 LSB <55	V <6.8	SB <104 μV	<5.5 LSB	<168 µV	<9.0 LSB	<550 μV	<6.8 LSB	<1.1 mV	<5.5 LSB	<1.7 mV
1 ΜΩ	<9.5 LSB <58	V <7.1	SB <109 μV	<5.5 LSB	<168 µV	<9.5 LSB	<580 μV	<7.1 LSB	<1.1 mV	<5.5 LSB	<1.7 mV

# Dynamic Parameters, typical figures

		M2p.592x, DN2.592-xx, DN6.592-xx										
Test - sampling rate		20 MS/s										
Input Range	±200 m\	±200 mV		) mV	±l	l	±2	V				
Test Signal Frequency	1 MHz	n.a.	.a. 1 MHz n.a.		1 MHz	n.a.	1 MHz	n.a.				
SNR (typ)	≥77.2 dB	n.a.	≥79.8 dB	n.a.	≥ 81.0 dB	n.a.	≥75.0 dB	n.a.				
THD (typ)	≤ 92.5 dB	n.a.	≤ -92.8 dB	n.a.	$\leq$ -89.5 dB	n.a.	≤ -76.5 dB	n.a.				
SFDR (typ), excl. harm.	≥ 103.0 dB	n.a.	$\geq$ 103.0 dB	n.a.	$\geq$ 105.0 dB	n.a.	$\geq$ 93.0 dB	n.a.				
ENOB (based on SNR)	≥ 12.5 LSB	n.a.	$\geq$ 13.0 LSB	n.a.	$\geq$ 13.2 LSB	n.a.	$\geq$ 12.2 LSB	n.a.				
ENOB (based on SINAD)	≥ 12.5 LSB	n.a.	$\geq$ 13.0 LSB	n.a.	$\geq 13.1 \text{ LSB}$	n.a.	$\geq$ 11.8 LSB	n.a.				

	M2p.593x, DN2.593-xx, DN6.593-xx									
Test - sampling rate		40 MS/s								
Input Range	±200	mV	±500	±500 mV		1	±2 V			
Test Signal Frequency	1 MHz	10 MHz	1 MHz	10 MHz	1 MHz	10 MHz	1 MHz	10 MHz		
SNR (typ)	≥73.0 dB	≥72.6 dB	≥74.6 dB	≥74.4 dB	≥75.3 dB	≥75.3 dB	≥71.9 dB	≥71.8 dB		
THD (typ)	≤ -87.8 dB	$\leq$ -67.0 dB	≤ -89.0 dB	$\leq$ -67.0 dB	≤-86.1 dB	$\leq$ -67.2 dB	≤ -79.0 dB	≤-67.2 dB		
SFDR (typ), excl. harm.	$\geq$ 98.3 dB	$\geq$ 96.5 dB	≥98.8 dB	$\geq$ 99.5 dB	$\geq$ 101.0 dB	$\geq 100.0 \text{ dB}$	≥ 81.7 dB	$\geq$ 91.3 dB		
ENOB (based on SNR)	$\geq 11.8$ LSB	$\geq 11.8$ LSB	$\geq$ 12.1 LSB	$\geq$ 12.0 LSB	$\geq$ 12.2 LSB	$\geq 12.2 \text{ LSB}$	≥ 11.7 LSB	$\geq$ 11.6 LSB		
ENOB (based on SINAD)	$\geq 11.8 \text{ LSB}$	$\geq 10.7 \; \text{LSB}$	$\geq$ 12.1 LSB	$\geq 10.7 \text{ LSB}$	$\geq$ 12.2 LSB	$\geq 10.8 \ \text{LSB}$	$\geq$ 11.6 LSB	$\geq 10.7 \; \text{LSB}$		

		M2p.594x								
Test - sampling rate		80 MS/s								
Input Range	±200	) mV	±500	±500 mV		±1		V		
Test Signal Frequency	1 MHz	10 MHz	1 MHz	10 MHz	1 MHz	10 MHz	1 MHz	10 MHz		
SNR (typ)	≥70.6 dB	$\geq$ 70.5 dB	≥72.9 dB	≥72.8 dB	≥74.2 dB	$\geq$ 74.2 dB	≥ 69.8 dB	≥69.8 dB		
THD (typ)	$\leq$ -87.3 dB	$\leq$ -76.9 dB	≤ -86.6 dB	$\leq$ -76.3 dB	$\leq$ -84.8 dB	$\leq$ -70.1 dB	≤ -79.0 dB	≤ -77.9 dB		
SFDR (typ), excl. harm.	≥ 97.5 dB	$\geq 105.0 \text{ dB}$	$\geq$ 101.0 dB	$\geq$ 104.0 dB	$\geq$ 100.0 dB	$\geq$ 100.0 dB	≥ 96.9 dB	$\geq$ 96.6 dB		
ENOB (based on SNR)	$\geq 11.4$ LSB	$\geq 11.4$ LSB	$\geq$ 11.8 LSB	$\geq$ 11.8 LSB	$\geq$ 12.0 LSB	$\geq$ 12.0 LSB	$\geq$ 11.2 LSB	$\geq 11.2 \text{ LSB}$		
ENOB (based on SINAD)	$\geq 11.4$ LSB	$\geq 11.3 \ \text{LSB}$	$\geq$ 11.8 LSB	$\geq 11.5 \text{ LSB}$	$\geq$ 12.0 LSB	$\geq$ 11.1 LSB	$\geq$ 11.2 LSB	$\geq 11.2 \ \text{LSB}$		

	M2p.596x, DN2.596-xx, DN6.596-xx												
Test - sampling rate		125 MS/s											
Input Range		±200 mV			±500 mV			±1V			±2 V		
Test Signal Frequency	1 MHz	10 MHz	40 MHz	1 MHz	10 MHz	40 MHz	1 MHz	10 MHz	40 MHz	1 MHz	10 MHz	40 MHz	
SNR (typ)	≥68.1 dB	≥66.2 dB	≥65.5 dB	≥70.5 dB	≥ 69.9 dB	≥ 68.7 dB	≥73.3 dB	≥72.7 dB	≥71.5 dB	≥67.8 dB	≥65.8 dB	≥65.1 dB	
THD (typ)	≤ -81.5 dB	≤-74.5 dB	≤-53.7 dB	≤-82.5 dB	≤-77.6 dB	$\leq$ -55.3 dB	$\leq$ -83.3 dB	$\leq$ -68.9 dB	≤-57.3 dB	≤-78.0 dB	≤-75.6 dB	≤-53.7 dB	
SFDR (typ), excl. harm.	$\geq$ 95.0 dB	$\geq$ 93.4 dB	$\geq$ 92.3 dB	$\geq 97.5 \text{ dB}$	$\geq$ 96.8 dB	$\geq$ 94.0 dB	≥ 98.5 dB	$\geq$ 98.1 dB	$\geq$ 96.4 dB	≥91.5 dB	$\geq$ 89.0 dB	$\geq$ 89.0 dB	
ENOB (based on SNR)	$\geq$ 11.0 LSB	$\geq 10.7 \text{ LSB}$	$\geq 10.6$ LSB	$\geq$ 11.4 LSB	$\geq$ 11.3 LSB	≥ 11.1 LSB	$\geq 11.8$ LSB	$\geq 11.8$ LSB	≥ 11.6 LSB	$\geq$ 11.0 LSB	$\geq 10.6 \text{ LSB}$	$\geq 10.5 \text{ LSB}$	
ENOB (based on SINAD)	$\geq$ 11.0 LSB	$\geq 10.6 \text{ LSB}$	$\geq$ 8.6 LSB	$\geq$ 11.4 LSB	$\geq$ 11.1 LSB	$\geq$ 8.9 LSB	$\geq 11.7$ LSB	$\geq 11.0$ LSB	$\geq$ 9.2 LSB	$\geq 10.9 \text{ LSB}$	$\geq 10.6 \text{ LSB}$	$\geq$ 8.6 LSB	

Dynamic parameters are measured at  $\pm 1$  V input range (if no other range is stated) and 50 $\Omega$  termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave generated by a signal generator and a matching bandpass filter. Amplitude is >99% of FSR. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits.

# **DN6 specific Technical Data**

### Environmental and Physical Details DN6.xxx

Dimension of Chassis without connectors or bumpe	rs LxWxH	464 mm x 431 mm x 131 mm
Dimension of Chassis with 19" rack mount option	L x W x H	464 mm x TBD mm x 131 mm (3U height)
Weight (3 internal acquisition/generation modules	)	12.1 kg, with rack mount kit: TBD kg
Weight (4 internal acquisition/generation modules	)	12.5 kg, with rack mount kit: TBD kg
Weight (5 internal acquisition/generation modules	)	12.9 kg, with rack mount kit: TBD kg
Weight (6 internal acquisition/generation modules	)	13.4 kg, with rack mount kit: TBD kg
Warm up time		10 minutes
Operating temperature		0°C to 40°C
Storage temperature		-10°C to 70°C
Humidity		10% to 90%
Dimension of packing (single DN6)	L x W x H	580 mm x 580 mm x 280 mm
Volume weight of Packing (single DN6)		19.0 kgs

### **Power Consumption**

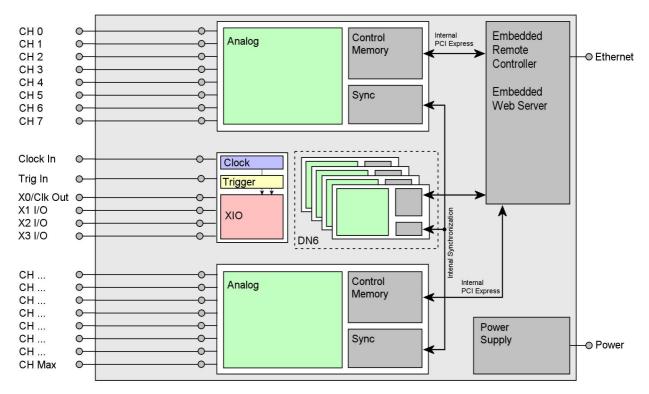
	230 VA	с
24 channel versions, standard memory	TBD	TBD
32 channel versions, standard memory	TBD	TBD
40 channel versions, standard memory	TBD	TBD
48 channel versions, standard memory	TBD	TBD

#### <u>MTBF</u>

MTBF

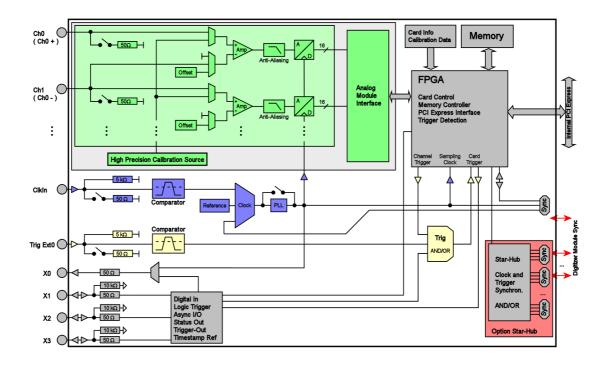
TBD hours

# **Block diagram of digitizerNETBOX DN6**



• The number of maximum channels and internal digitizer modules and existance of a synchronization Star-Hub is model dependent.

# **Block diagram of digitzerNETBOX module DN6.59x**



# **Order Information**

The digitizerNETBOX is equipped with a large internal memory for data storage and supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, ABA mode and Timestamps. Operating system drivers for Windows/Linux 32 bit and 64 bit, drivers and examples for C/C++, IVI (Scope and Digitizer class), LabVIEW (Windows), MATLAB (Windows and Linux), LabWindows/CVI, .NET, Delphi, Java, Python and a Professional license of the oscilloscope software SBench 6 are included.

The system is delivered with a connection cable meeting your countries power connection. Additional power connections with other standards are available as option.

Order no.	A/D Resolution	Bandwidth	Memory	Single-Ended Inputs	Differential Inputs	
DN6.592-24	16 Bit	10 MHz	3 x 512 MSamples	24 channels 20 MS/s	12 channels 20 MS/s	
DN6.592-32	16 Bit	10 MHz	4 x 512 MSamples	32 channels 20 MS/s	16 channels 20 MS/s	
DN6.592-40	16 Bit	10 MHz	5 x 512 MSamples	40 channels 20 MS/s	20 channels 20 MS/s	
DN6.592-48	16 Bit	10 MHz	6 x 512 MSamples	48 channels 20 MS/s	24 channels 20 MS/s	
DN6.593-24	16 Bit	20 MHz	3 x 512 MSamples	24 channels 40 MS/s	12 channels 40 MS/s	
DN6.593-32	16 Bit	20 MHz	4 x 512 MSamples	32 channels 40 MS/s	16 channels 40 MS/s	
DN6.593-40	16 Bit	20 MHz	5 x 512 MSamples	40 channels 40 MS/s	20 channels 40 MS/s	
DN6.593-48	16 Bit	20 MHz	6 x 512 MSamples	48 channels 40 MS/s	24 channels 40 MS/s	
DN6.596-24	16 Bit	60 MHz	3 x 512 MSamples	12 channels 125 MS/s 24 channels 80 MS/s	12 channels 125 MS/s	
DN6.596-32	16 Bit	60 MHz	4 x 512 MSamples	16 channels 125 MS/s 32 channels 80 MS/s	16 channels 125 MS/s	
DN6.596-40	16 Bit	60 MHz	5 x 512 MSamples	20 channels 125 MS/s 40 channels 80 MS/s	20 channels 125 MS/s	
DN6.596-48	16 Bit	60 MHz	6 x 512 MSamples	24 channels 125 MS/s 48 channels 80 MS/s	24 channels 125 MS/s	

#### digitizerNETBOX DN6 - Ethernet/LXI Interface

#### **Options**

Order no.	Option
DN6.xxx-Rack	19" rack mounting set for self mounting
DN6.xxx-Emb	Extension to Embedded Server: CPU, more memory, SSD. Access via remote Linuxs secure shell (ssh)
DN6.xxx-BTPWR	Boot on Power On: the digitizerNETBOX/generatorNETBOX automatically boots if power is switched on.

#### **BNC Cables**

The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz.

for Connections	Connection	Length	to SMA male	to SMA female	to BNC male	to SMB female	
All	BNC male	80 cm	Cab-9m-3mA-80	Cab-9m-3fA-80	Cab-9m-9m-80	Cab-9m-3f-80	
All	BNC male	200 cm	Cab-9m-3mA-200	Cab-9m-3fA-200	Cab-9m-9m-200	Cab-9m-3f-200	

#### Technical changes and printing errors possible

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