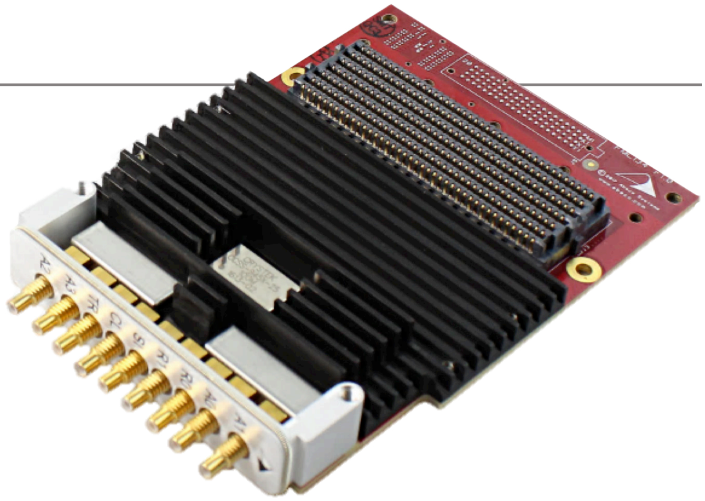


FMC134 FPGA Mezzanine Card

Direct RF conversion module

The FMC134 provides customers with a high bandwidth and high channel count I/O solution that is ideal for multi-channel receivers in a wide range of applications.

With four 12-bit analog-to-digital channels up to 3.2GSPS or two analog channels up to 6.4GSPS, the FMC134's design is based on the Texas Instruments™ ADC12DJ3200 and is mechanically and electrically compliant with the FMC+ standard (VITA 57.4), the next generation of small form factor expansion I/O for high performance FPGA-based systems.

The A/D JESD204B data interface connects to an FPGA using 16 of the 24 high speed serial lanes available on an FMC+ high serial pin count (HSPC) connector. The unused eight high speed serial lanes are passed to the top of the board, enabling the potential for FMC stacking.

The sample clock can be supplied externally through a coax connection or supplied by an internal clock source (optionally locked to an external reference) for multi-board and multi-channel synchronization.

The board also includes an external trigger input and two reference outputs that can be enabled for multi-board synchronization.

The front panel I/O can optionally be populated with MMCX or SSMC coaxial connectors. Analog I/O is AC-coupled.

When paired with the latest FPGA carrier cards with FMC+ sites - such as the Abaco VP880 or the VP868 with Xilinx® Ultrascale™ technology - customers can implement high performance algorithms on an industry standard platform.

Applications include:

- Traditional radar
- Bi-static radar
- Multi-channel radar
- Wideband receivers
- Wireless communication SDR applications
- Signals intelligence receiver

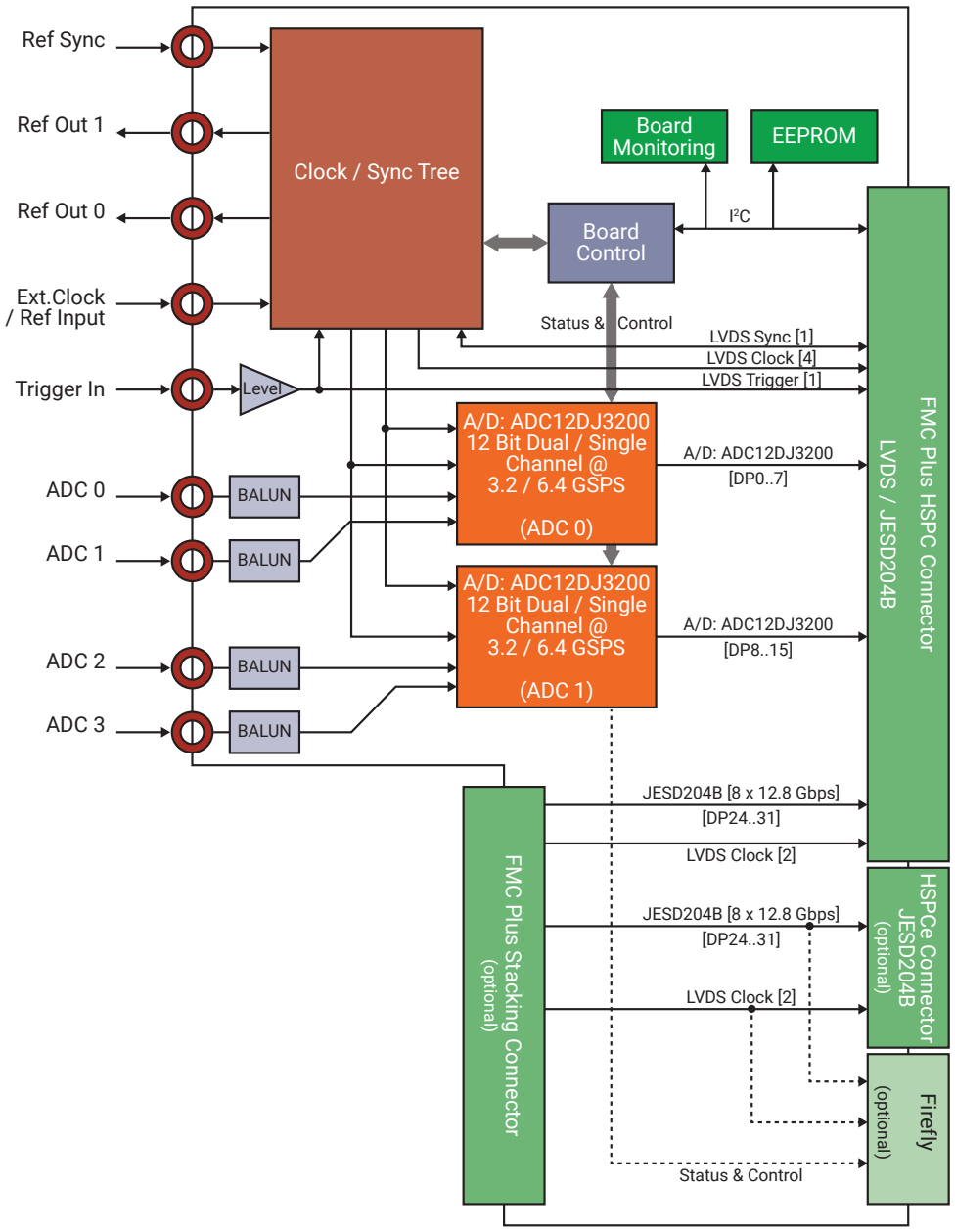
FEATURES:

- Two operational modes
  - 4 channels, 12-bit, 3.2GSPS data rate
  - 2 channels, 12-bit, 6.4GSPS data rate
- VITA 57.4 HSPC FMC+ site required
- 16 JESD204B lanes at 12.8GBPS
- 8 JESD204B lanes passed to board topside for FMC stacking
- Optional FMC+e connection for additional stacked serial lanes
- Conduction cooled configuration available
- AC-coupled analog input
- 9 front panel SSMC or MMCX connectors
- Internal or external clock
- MIL-I-46058c conformal coating (optional)
- 2Kbit EEPROM (M24C02-WDW) accessible from the host via I2C bus
- Full-featured board support package.
  - Open source VHDL reference design
  - Open source C/C++ reference examples. Windows® and Linux® support.
  - JESD204B core included
  - Simplified IP integration with StellarIP

abaco SYSTEMS

FMC134 FPGA Mezzanine Card *Direct RF conversion module*

Block diagram



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