

VP431

3U VPX Direct RF Processing System with Xilinx Zynq Ultrascale+ RFSoc Gen3

The VP431 is a 3U VPX RF processing system featuring the 3rd generation of the transformational Xilinx® Zynq® Ultrascale+™ RF system-on-chip technology (RFSoc). The ZU47DR device used on the VP431 includes eight integrated analog-to-digital converters sampling up to 5.0GSPS, eight digital-to-analog converters up to 10.0GSPS, a user programmable FPGA fabric, and multi-core Zynq ARM® processing subsystem. The VP431 is aligned with the Sensor Open Systems Architecture™ (SOSA) technical standard and also supports limited distribution options for enhanced performance.

Reduce RF Signal Chain Complexity

RF systems with multiple channels suffer from a cost- and complexity challenge. 'More channels' means more expensive and large RF signal up/down conversion and signal conditioning. As a solution, the VP431 enables direct RF sampling which can be processed in the digital domain, bringing greater flexibility to the signal processing chain. Additionally, close integration with RF sampling devices removes the complexity of JESD204B/C high-speed serial interfaces and reduces processing latency.

Maximize Input/Output Channel Density

The VP431 is one of the densest 3U VPX analog FPGA processing boards available with the ability to synchronize all 16 channels and across multiple boards for even larger system applications. Earlier generations would have taken four times as many boards.

Heterogeneous processing capability

Many RF and signal processing systems require both a streaming DSP with an FPGA and a general-purpose processor for decisions and control. In the past, these processing requirements were handled by separate modules. Now, with the VP431, it is possible to get both functions in a single module by leveraging application and real-time processing ARM cores as part of the RFSoc technology.

Offload Data More Efficiently

The VP431 has VPX backplane interfaces aligned with the SOSA RF payload slot profile, supporting 40 Gigabit Ethernet data plane, PCIe Gen3 x4 expansion plane and Gigabit Ethernet control plane connections to a host computer or other payloads. With eight ADCs sampling at rates up to 5GSPS, or higher with the limited distribution device, and two bytes per sample, even these modern high-speed data connections are too slow for a direct transfer. To overcome this challenge, the VP431 is available with an optional dual channel 100 Gigabit Ethernet fiber optic interface for transfers up to 25 GB/s.

The VP431 is available with two cooling options, air or conduction, making it an ideal COTS product for early designs and capable of being deployed into operational assets. When paired with Abaco's extensive portfolio of multi-architecture processing boards including SBCs, GPGPUs, and fabric switches the state-of-the-art VP431 enables systems to be built from leading edge, interoperable components.

FEATURES:

- Zynq UltraScale+ RFSoc
 - Integrated ADC, DAC, programmable logic and processing subsystems
- ADC 8-channel >5.0GSPS 14-Bit
- DAC 8-channel 10.0GSPS 14-Bit
- Flexible ADC/DAC clocking scheme
 - Dual PLL for independent ADC channel clocking
- Expanded Decimation and Interpolation Options
- Application Processing Unit
 - Quad-core ARM Cortex-A53
- Real-time Processing Unit
 - Dual-core ARM Cortex-R5
- Up to 16 GBytes DDR4
- FireFly™ Gen2 Optical Transceivers option
- I/O
 - 10/40G Ethernet (provision for 25/100G Ethernet over copper in the future)
 - PCIe Gen3 x4
 - Gigabit Ethernet
 - Dual 100G Ethernet optical
 - 20 RF-to-backplane (NanoRF)
 - 8 LVDS GPIO
- Aligned to SOSA standard
- Air-Cooled / Conduction Cooled configurations available
- MIL-I-46058C compliant conformal coating (optional)

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Physical Specifications

- 3U VPX 1.0" pitch
- Air-cooled or conduction cooled

SOSA RF Payload Slot Profile

- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n

Zynq Ultrascale+ RFSoc Gen3

- ZU47DR or limited distribution device

Memory

- Two 64-bit 8GBytes DDR4 (16GB total) memory blocks; up to 2400 Mb/s
- RFSoc - 256KB on-chip with ECC

ADC and DAC

- ADC: 8-channels, 14-bit, 5.0GSPS with DDC (>5.0GSPS with limited distribution device)
- DAC: 8-channels, 14-bit, 10.0GSPS with DUC

Programmable FPGA Logic

- 930k System Logic Cells
- 425k CLB LUTs
- 4,272 DSP Slices

Application Processing Unit

- Quad-core ARM Cortex-A53 MPCore
- Up to 1.33GHz

Real-time Processing Unit

- Dual-core ARM Cortex-R5 MPCore
- Up to 533MHz

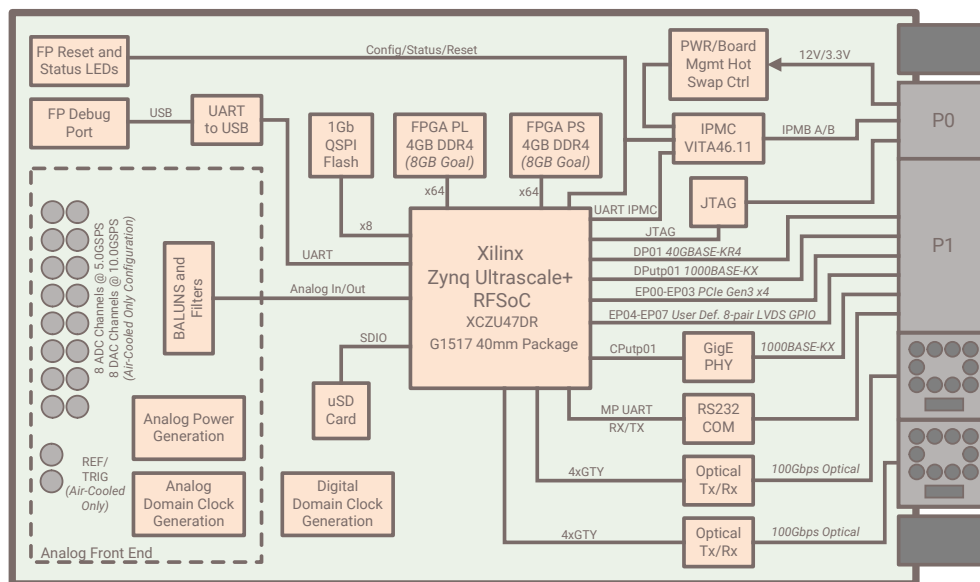
Flexible RF/Optical Backplane Options

- Dual NanoRF 10 port connector option in conduction cooled for ADC/DAC/CLK/TRIG
- Dual 4-lane bidirectional optical interface via FireFly Gen2 (optional) - 100G Ethernet or Aurora independent channels up to 25 GB/s

Operating Temperature

- 0°C to +55°C (Level 1 air-cooled environment with 400 LFM mean airflow)
- -40°C to +70°C (Level D conduction-cooled environment at the card thermal interface)

Block diagram



Ordering information

For available product part numbers, contact your local product expert.

Board Support Package (BSP)

- Open Source access to most of the firmware
 - 40G Ethernet with RoCEv2 (RDMA over Converged Ethernet) available
 - Xilinx PCIe DMA engine included
 - 100Gbps Aurora or 100G Ethernet over optical interface available
 - Optional ANSI/VITA 49.2 VITA Radio Transport (VRT) subset protocol support for Software Defined Radios
- Open source Windows and Linux API
- For VxWorks, please contact Abaco Systems

Applications

- Direct RF Down Conversion
- Electronic Warfare (EW)
- Signal Intelligence (SIGINT)
- Radar/Sonar
- Software Defined Radio (SDR)
- Multi-Function Communication Systems
- Broadband Wireless
- Networking and Base Stations Equipment
- Ultra-Wide-Band Satellite Digital Receiver
- Optical and Photonics Instrumentation
- RF and EMI Test Instrumentation
- Biomedical Imaging – Medical Equipment

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