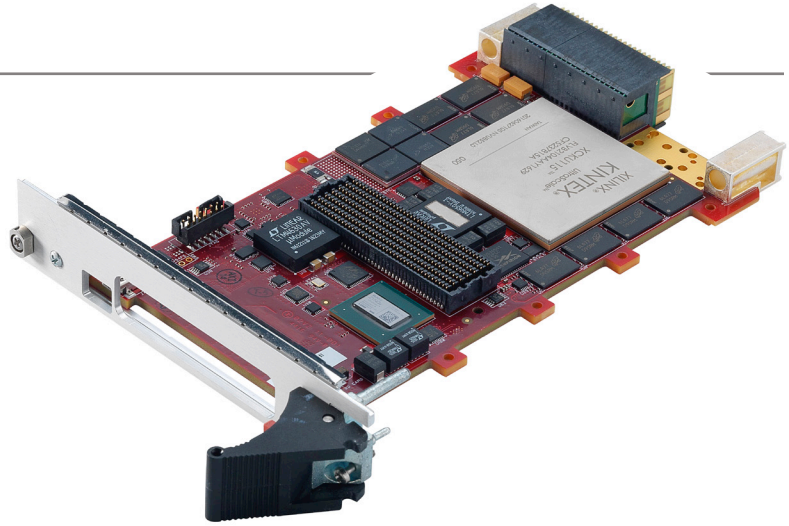


VP880 Ultrascale FPGA, Zynq Ultrascale+ and FMC+

3U OpenVPX FPGA Card

The VP880 is a high-performance FPGA processing board featuring Xilinx® Ultrascale™ and Zynq® Ultrascale+™ technology. It is designed for the most demanding, mission critical military/defense applications such as electronic warfare/ DRFM, radar/sonar image processing, satellite communications systems, multi-channel digital transmission/reception and advanced digital beamforming.

Upgradability built in

With seven Ultrascale FPGAs to choose from, as well as a migration path to a range of Virtex™ Ultrascale+ devices, the VP880 brings high performance, flexibility, and longevity to the 3U VPX form factor. In line with Abaco's commitment to maximizing return on customer investment and minimizing long term cost of ownership, the VP880 mitigates the impact of obsolescence for existing or future customers by allowing for rapid migration to future FPGA devices, while its adherence to industry standards assures both flexibility and longevity.

Secure

The Zynq Ultrascale+ system-on-chip (SoC) brings advanced security to the forefront. The VP880 is capable of advanced encrypted bit streams and secure boot capability, enabled by Xilinx tools. This makes it an ideal tool for applications where IP security is a top concern.

Flexibility you need for the system you want

Including the Zynq MPSoC removes the need for a single board computer in some applications, providing customers an efficient way to maximize system performance while reducing complexity.

The VITA 57.4 compliant FMC+ site allows users to take advantage of Abaco's industry-leading FMC I/O portfolio. Modular I/O built on an FMC+ standard interface enables engineers to easily upgrade to future technology without a complete system redesign.

The VP880 includes flexible VPX backplane options with VITA 67.1 and VITA 67.2 analog interface ports. Optionally, the VP880 can be configured to support 12 optical FireFly™ RX/TX lanes mapped to a VITA 66.4 backplane interface.

The VP880 is offered in its default configuration with full BLAST support and multiple VITA 67 backplane options. An extended backplane IO version is available (EG. VP881) that adds additional backplane LVDS and MGT resources, added VITA 46.6 UTP-2 Support for 10GBASE-KR, and removes support for traditional BLAST and VITA 67.2.

Typical applications

- Electronic Warfare
- ISR
- Radar Signal Processing
- Software Defined Radio

FEATURES:

- Dual FPGA architecture
  - Kintex or Virtex Ultrascale
  - Zynq Ultrascale+ MPSoC
- 8GB DDR4 mapped to FPGA
- 2GB DDR4 mapped to Zynq
- VITA 57.4 HSPC FMC+ site interfacing with the Ultrascale FPGA
- Conduction Cooled Configuration Available
- VITA 66.4 optical interface via FireFly BLAST site
- Up to two COM ports from the Zynq to the backplane
- 1 GB Ethernet PHY to Backplane
- Front Panel USB UART
- USB 3.0, SATA 3.0, Display Port to Backplane RTM
- VPX Back plane GPIO
- I2C Interface P0 to Zynq
- Operating system support
  - Linux®
  - Windows®
  - VxWorks®
- Full-featured Board Support Package (BSP)
  - Open VHDL reference design
  - Open C/C++
  - PCIe™ core included with BSP
  - Peta Linux® reference design

abaco SYSTEMS

VP880 *Ultrascale FPGA, Zynq Ultrascale+ and FMC+ 3U OpenVPX FPGA Card*

Specifications

Build options
- 0.8" pitch convection cooled
- 1.0" pitch conduction cooled

Virtex Ultrascale options
- XCVU080
- XCVU095
- XCVU125
- XCVU160
- XCVU190

Kintex Ultrascale options
- XCKU095
- XCKU115

Zynq Ultrascale+ MPSoC
- XCZU3EG

Memory
- 8GB DDR4 mapped to FPGA
- 2GB DDR4 mapped to Zynq

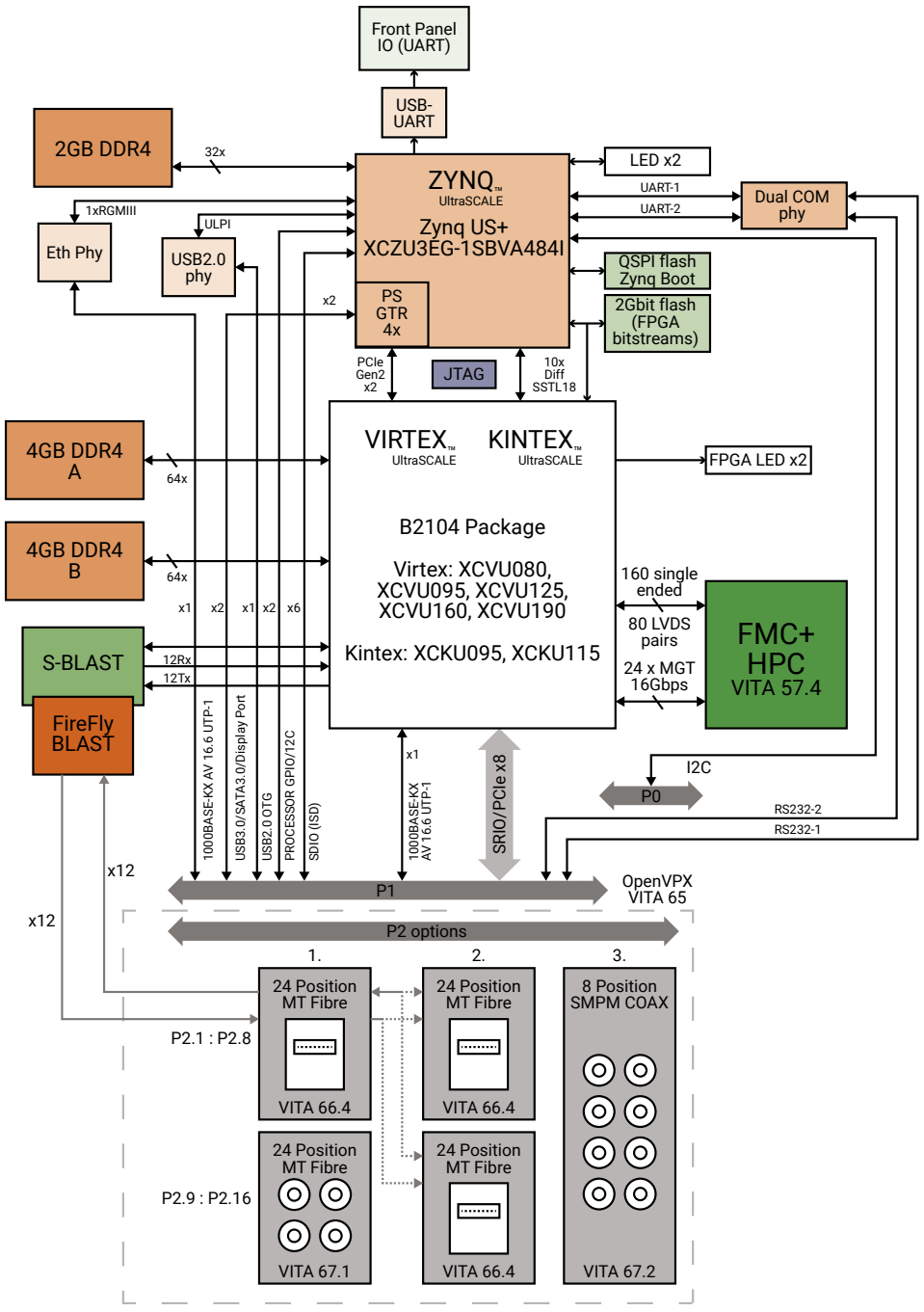
Analog and/or digital
- 1x HSPC FMC+ site
- Configurable with Abaco's FMC portfolio

Flexible VPX backplane options
- VITA 67.1 and VITA 67.2 analog interface ports
- VITA 66.4 Optical Interface via FireFly BLAST site (optional)

Supported OpenVPX slot profiles
- SLT3-PAY-2F1F2U-14.2.1
- SLT3-PAY-1F2F2U-14.2.2
- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PAY-1F2U-14.2.12
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

Additional slot profiles are available depending on your configuration. Contact sales for more information.

VP880 Block diagram



VP880 *Ultrascale FPGA, Zynq Ultrascale+ and FMC+ 3U OpenVPX FPGA Card*

Specifications

Build options
- 0.8" pitch convection cooled
- 1.0" pitch conduction cooled

Virtex Ultrascale options
- XCVU080
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- XCVU125
- XCVU160
- XCVU190

Kintex Ultrascale options
- XCKU095
- XCKU115

Zynq Ultrascale+ MPSoC
- XCZU3EG

Memory
- 8GB DDR4 mapped to FPGA
- 2GB DDR4 mapped to Zynq

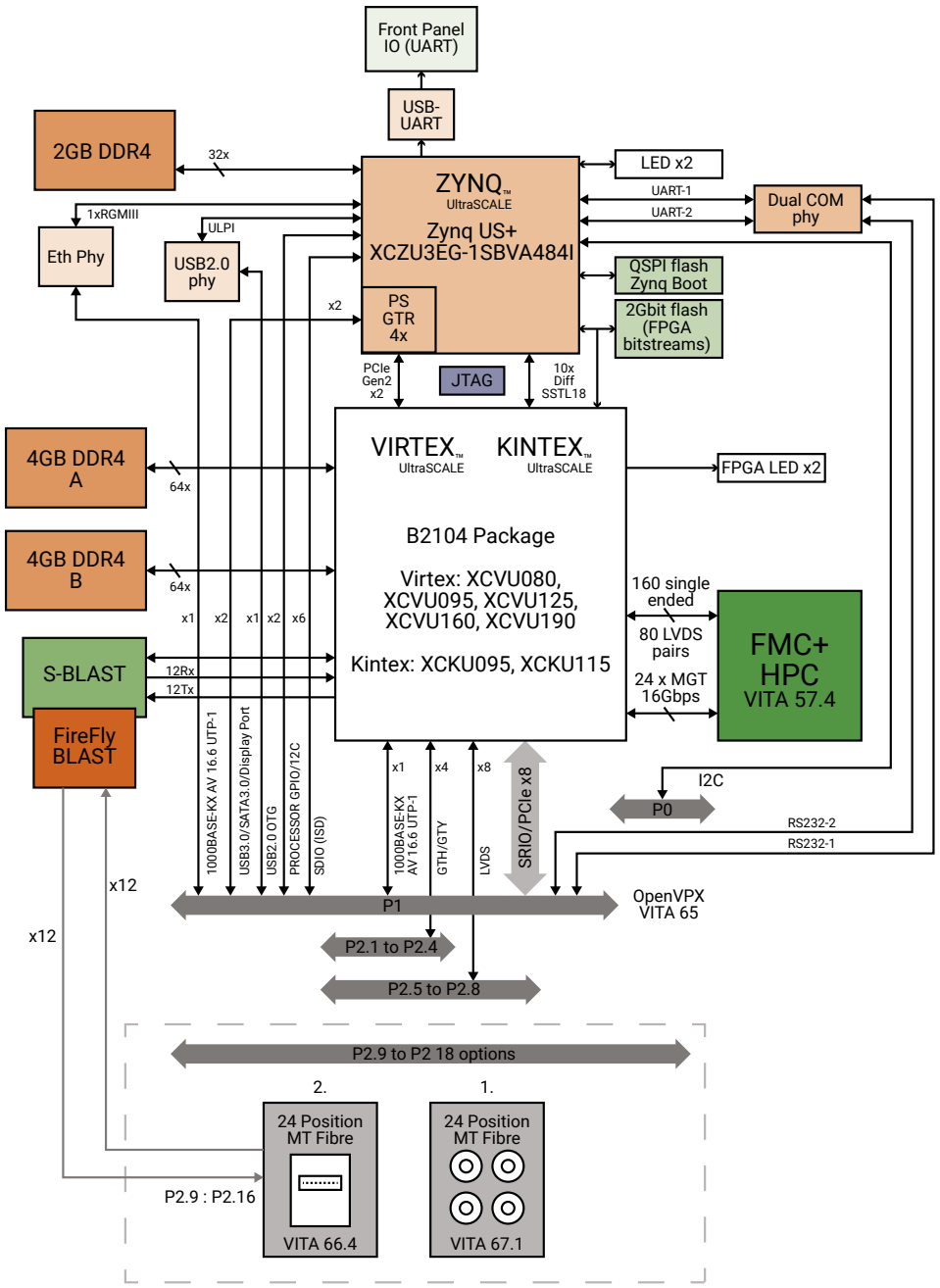
Analog and/or digital
- 1x HSPC FMC+ site
- Configurable with Abaco's FMC portfolio

VP881 Expanded VPX Backplane Options
- VITA 67.1 analog interface ports
- VITA 66.4 optical interface via FireFly BLAST site (optional)
- VITA 46.6 UTP-2 Support For 10GBASE-KR
- Added I/O on VPX P2.1 to P2.8 Differential I/O
  - 4x MGT / GTX I/O Mapped (P2.1 to P2.4)
  - 4x LVDS Signals (P2.5 to P2.8)
- Traditional BLAST and VITA 67.2 Not Supported

Supported OpenVPX slot profiles
- SLT3-PAY-2F1F2U-14.2.1
- SLT3-PAY-1F2F2U-14.2.2
- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PAY-1F2U-14.2.12
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

Additional slot profiles are available depending on your configuration. Contact sales for more information.

VP881 – Extended Backplane I/O Option Block diagram



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