

VP889 Virtex UltraScale+ FPGA, Zynq UltraScale+ and FMC+ 3U OpenVPX FPGA Card

The VP889 is a high-performance FPGA processing board featuring Xilinx® Virtex UltraScale+™ and Zynq® UltraScale+™ technology. A form, fit and function upgrade for the VP881, it is designed for the most demanding, mission critical military/defense applications such as electronic warfare/DRFM, radar/sonar processing, satellite communications systems, multi-channel digital transmission/reception and advanced digital beamforming.

Secure

The Zynq UltraScale+ system-on-chip (SoC) brings advanced security to the forefront. The VP889 is capable of advanced encrypted bit streams and secure boot capability, enabled by Xilinx tools. This makes it an ideal tool for applications where IP security is a top concern.

The flexibility you need for the system you want

Including the Zynq MPSoC removes the need for a single board computer in some applications, providing customers an efficient way to maximize system performance while reducing complexity.

The VITA 57.4-compliant FMC+ site allows users to take advantage of Abaco's industry-leading FMC I/O portfolio. Modular I/O built on an FMC+ standard interface enables engineers to easily upgrade to future technology without a complete system redesign.

The VP889 includes flexible VPX backplane options with VITA 67.1 analog interface ports and support for 12 optical FireFly™ RX/TX lanes mapped to a VITA 66.4 backplane interface.

Typical applications

- Electronic Warfare
- ISR
- Radar Signal Processing
- Software Defined Radio

FEATURES:

- Dual FPGA architecture
 - Virtex UltraScale+
 - Zynq UltraScale+ MPSoC
- 8GB DDR4 mapped to FPGA
- 2GB DDR4 mapped to Zynq
- VITA 57.4 HSPC FMC+ site interfacing with the UltraScale FPGA
- Conduction cooled configuration available
- VITA 66.4 optical interface via FireFly BLAST site
- Up to two COM ports from the Zynq to the backplane
- 1 GB Ethernet PHY to backplane
- Front panel USB UART
- SATA 3.0, DisplayPort to backplane RTM
- VPX backplane GPIO
- I2C interface P0 to Zynq
- Operating system support
 - Linux®
 - Windows®
 - VxWorks®
- Full-featured Board Support Package (BSP)
 - Open VHDL reference design
 - Open C/C++
 - PCIe™ core included with BSP
 - Peta Linux® reference design

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Specifications

Build options

- 0.8" pitch convection cooled
- 1.0" pitch conduction cooled

Virtex Ultrascale options

- XCVU5P
- XCVU9P

Zynq Ultrascale+ MPSoC

- XCZU3EG

Memory

- 8GB DDR4 mapped to FPGA
- 2GB DDR4 mapped to Zynq

Analog and/or digital

- 1x HSPC FMC+ site
- Configurable with Abaco's FMC portfolio

VPX Backplane Options

- VITA 67.1 analog interface ports
- VITA 66.4 optical interface via FireFly BLAST site (optional)
- VITA 46.6 UTP-2 Support For 10GBASE-KR
- FPGA VPX I/O:
 - P1.1 to P1.8, 8x MGT up to 10.31 Gb/s
 - P2.1 to P2.4, 4x MGT up to 10.31 Gb/s
 - P2.5 to P2.8, 4x LVDS
- Traditional BLAST and VITA 67.2 Not Supported

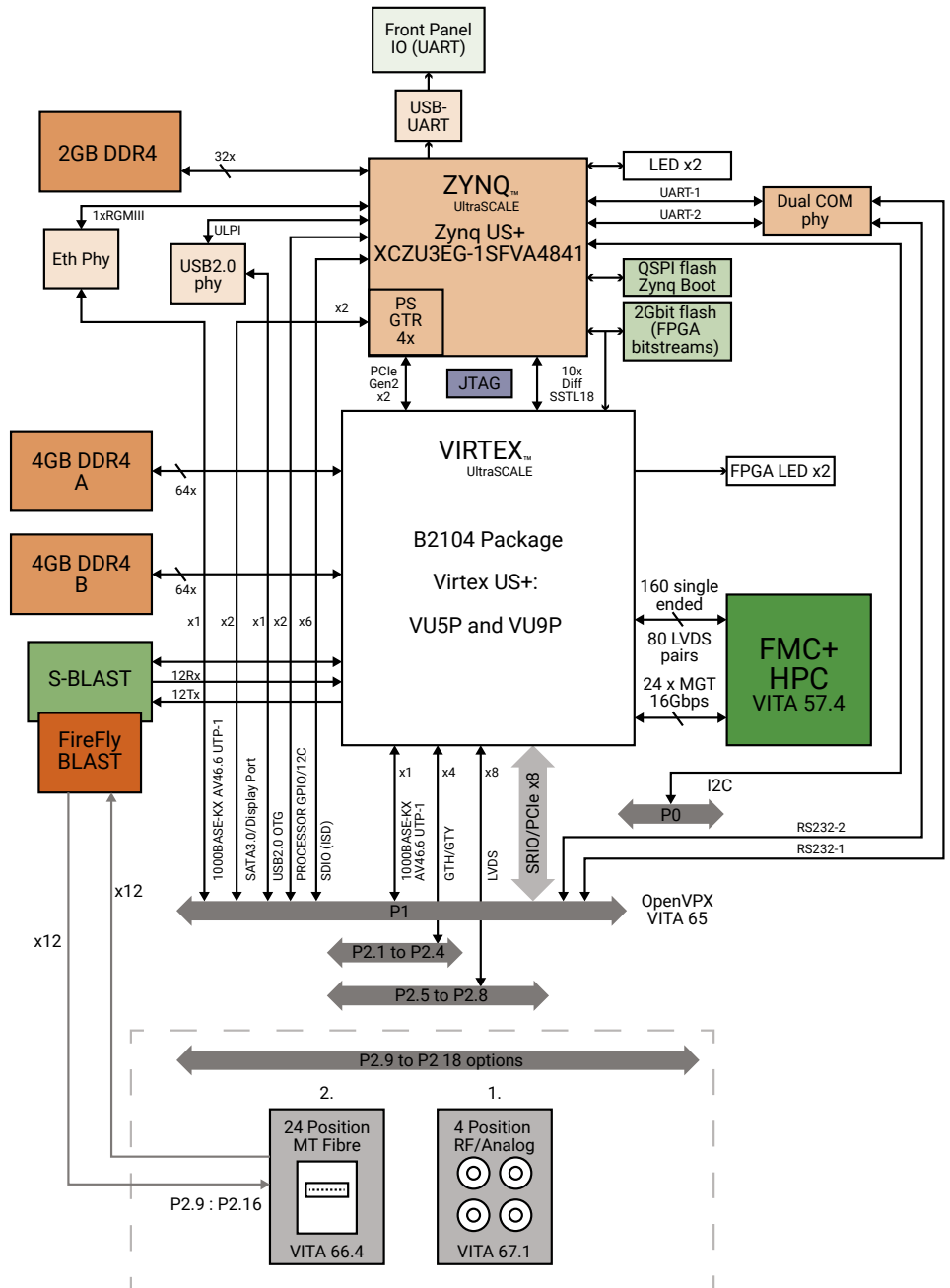
Supported OpenVPX slot profiles

- SLT3-PAY-2F1F2U-14.2.1
- SLT3-PAY-1F2F2U-14.2.2
- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9
- SLT3-PAY-1F2U-14.2.12
- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

Additional slot profiles are available depending on your configuration. Contact sales for more information.

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VP889 Block diagram



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